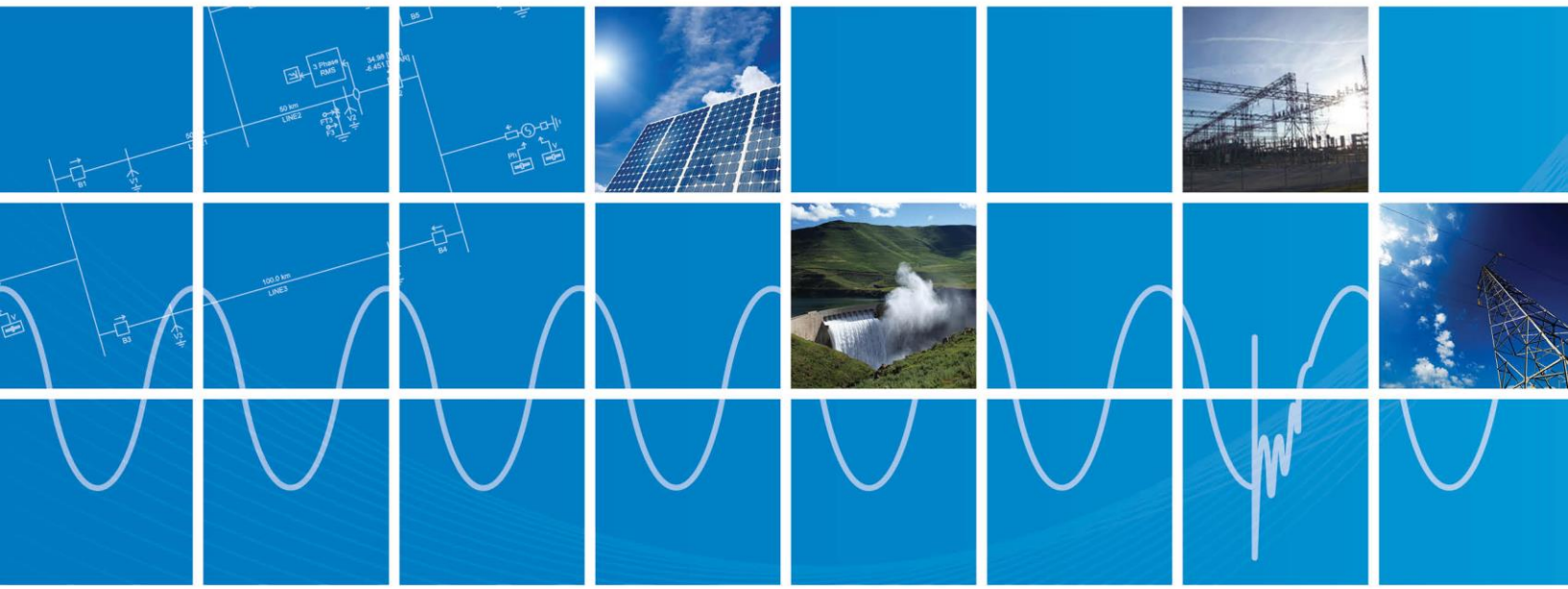
PSCAD Cookbook

Capacitor Bank Studies

Written for v4.5
Revision 1
May 08, 2018



Powered by Manitoba Hydro International Ltd.
211 Commerce Drive
Winnipeg, Manitoba
R3P 1A3 Canada
mhi.ca

Contents

2. CAPACITOR BANK STUDIES 1

2.1 CAPACITOR SWITCHING STUDY: ENERGIZING THE FIRST LEG OF A CAPACITOR BANK 1
2.2 BACK-TO-BACK CAPACITOR SWITCHING STUDY: TRANSIENT OVERVOLTAGE AND INRUSH CURRENT 10
2.3 CAPACITOR BANK DISCHARGE AND TRANSIENT OUTRUSH CURRENTS STUDY 19
2.4 VOLTAGE MAGNIFICATION DUE TO CAPACITOR SWITCHING TRANSIENTS STUDY 27
2.5 BREAKER POLE RESTRIKE PHENOMENA WITHIN A CAPACITOR BANK STUDY 34
2.6 TRANSFORMER PHASE-TO-PHASE OVERVOLTAGE STUDY 42

2. Capacitor Bank Studies

2.1 Capacitor Switching Study: Energizing the First Leg of a Capacitor Bank

Motivation

Capacitor banks are used in power systems to control bus voltages. The purpose of this study is to illustrate key points that need to be considered when the first leg of a capacitor bank is energized. In general, energizing a capacitor gives rise to fast transients.

The transient current that occurs when the capacitor bank is energized can be significantly higher than its rated current, and the frequency of the transient can reach a few kilohertz. The frequency, peak, and rate of change (i.e. $\frac{di}{dt}$) of the current must be controlled; this in order to ensure that the circuit breaker can withstand the capacitor energizing currents, without sustaining damage.

A variety of different events must be investigated in order to ensure the safe operation of circuit breakers at a capacitor bank installation. In this section, we look at the transients associated with energizing the first bank. This event is generally referred to as the *isolated switching* of a capacitor bank.

System Overview

In order to highlight the most basic aspects of isolated switching, the system is represented by a Thévanin voltage source, as shown in the simplified representation in Figure 1. Once the basic requirements for isolated switching are identified based on this simplified representation, it is advisable to perform a number of simulations in order to confirm that the switching conditions are acceptable. For this purpose, a more detailed representation of the system is recommended.

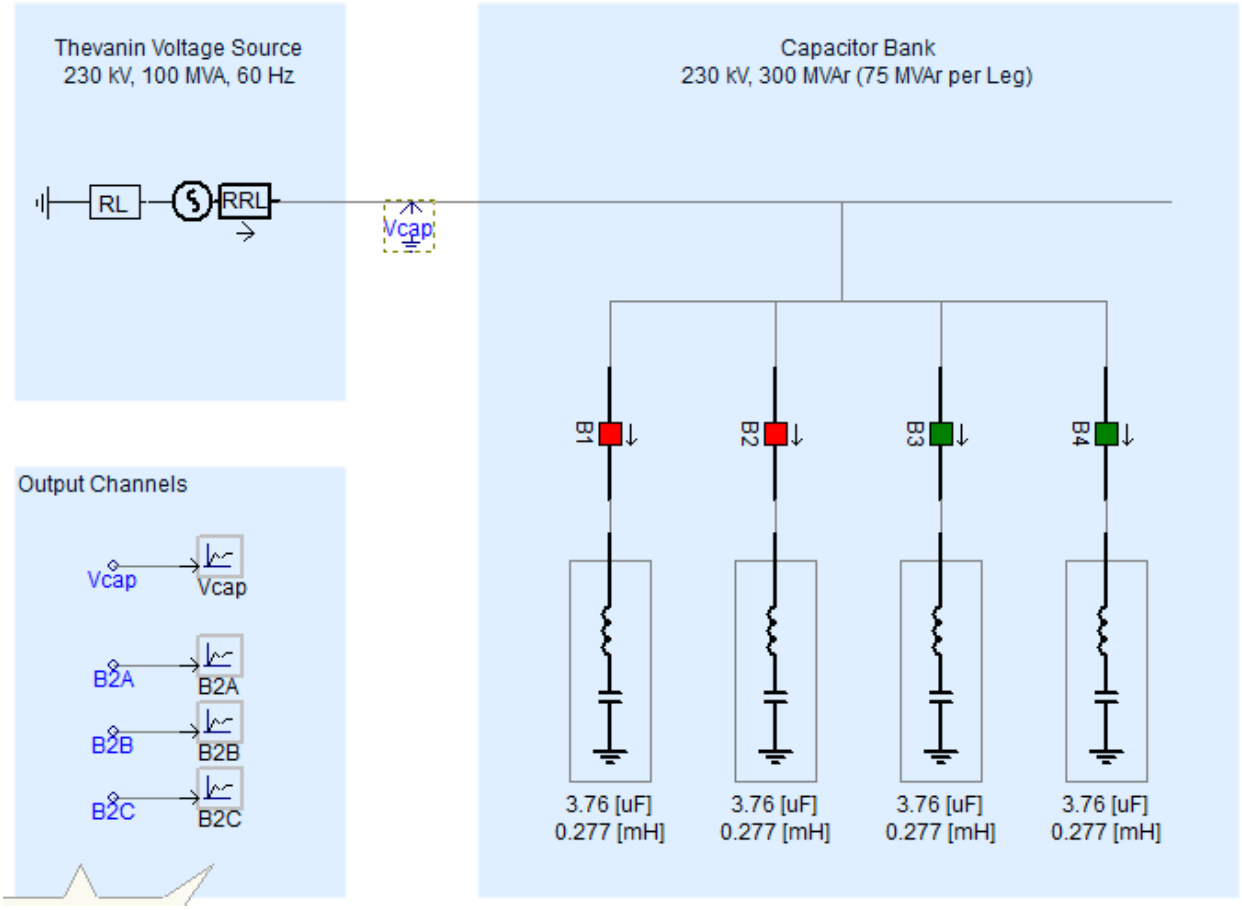


Figure 1: The 230 kV Source Connected to a 230 kV Capacitor Bank

The parameters of the voltage source, mainly the voltage magnitude, must correspond to the specific system operating condition. The worst case situation occurs when the bus voltage is at its maximum allowable value.

Enter the voltage source impedance corresponding to the fault level of the system, as measured from the capacitor bank location. This impedance, along with the capacitance of the first bank to be connected, will determine the nature of the current transient.[1]

The 230 kV capacitor bank is shown in Figure 2. The bank consists of four, 75 MVAr (25 MVAr per phase – 3.76 µF) capacitors. In this study, only one breaker (B1) is closed, thus energizing a single

[1] IEEE Standard 1036-2010, p. 27.

capacitor bank. All breakers are initially open; the other three breakers (B2, B3 and B4) remain open for the entire simulation.

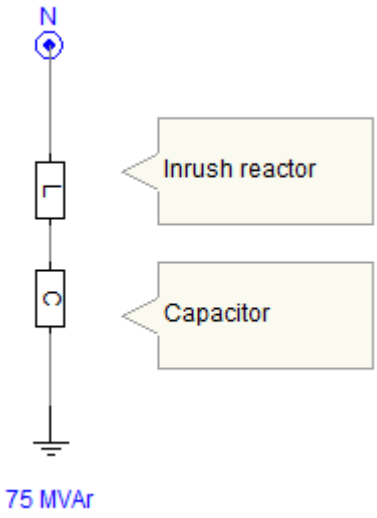


Figure 2: A Single Leg of the 230 kV Capacitor Bank (cap_bank_study_01_A.pscx)

A simplified circuit of a single phase is illustrated in Figure 3, in which the equivalent voltage maximum is represented by a 188 kV DC voltage source, corresponding to the peak value of a 230 kV AC supply.

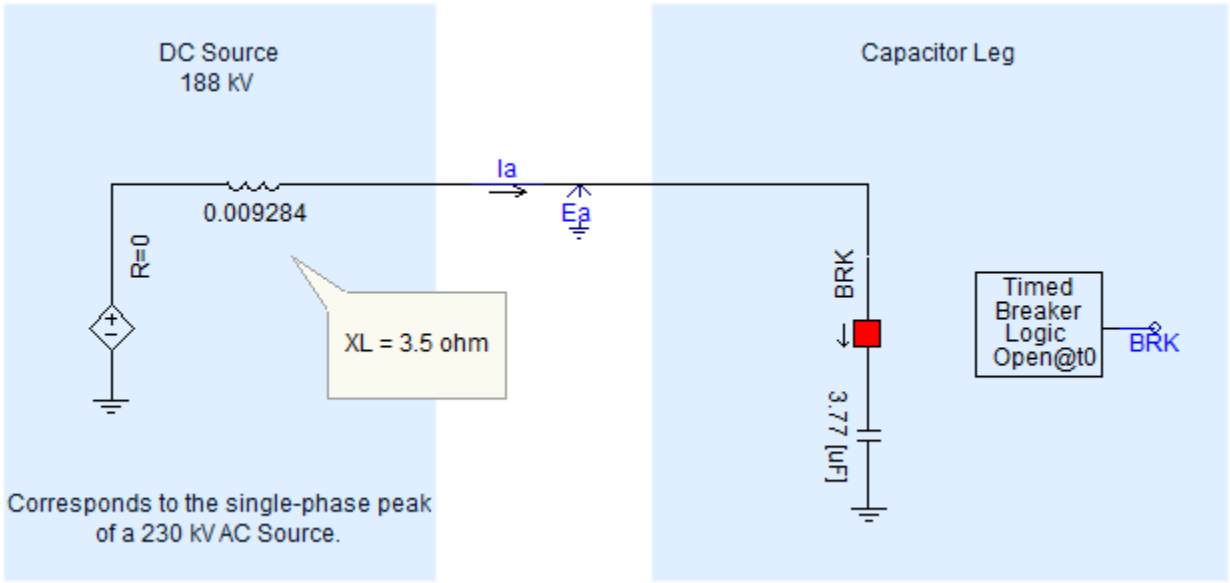


Figure 3: System Source Energizing a Single Leg of Capacitor Bank (cap_bank_study_01.B.pscx)

Energizing a capacitor from a predominately inductive source will give rise to transient currents, which will normally be of large magnitude and frequency. The actual response will be dependent on

the point on the voltage waveform at which the breaker is closed, as well as the surge impedance of the circuit.

The PSCAD 'Multiple-Run' component is used to time the instant at which the three poles of the circuit breaker are closed.

Analysis

The current flowing through the capacitor at normal power frequency is found to be 188.27 A:

$$I = \frac{Q}{\left(\sqrt{3} \cdot V\right)} = \frac{75 \times 10^6}{\left(\sqrt{3} \cdot 230k\right)} = 188.27\,A \qquad \text{2-1}$$

The capacitance for each leg can be determined via the following method:

$$X_c = \frac{V^2}{Q} \qquad \text{2-2}$$

$$C = \frac{Q}{V^2 \cdot \omega} = \frac{75 \times 10^6}{\left(230k\right)^2 \cdot 2\pi \cdot 60} = 3.76\,\mu F$$

The minimum source inductance required to limit the transient to an acceptable level is determined as follows. Assume that the rated (short-circuit) breaker current is 40 kA. Use a tolerance factor of 5 % for the voltage (V = 230 kV x 1.05).

$$X_L = \frac{V}{\left(\sqrt{3} \cdot 40k\right)} \approx 3.5\Omega \qquad \text{2-3}$$

$$L = \frac{X_L}{\omega} = \frac{3.5}{2\pi \cdot 60} = 0.00928\,H \qquad \text{2-4}$$

Thus if the system impedance, as determined by the fault level at the capacitor bus, is greater than 3.5 Ω, the isolated switching transients will not adversely impact the circuit breaker.

The following equations can be used to determine the magnitude and frequency of the inrush currents when breaker B1 is closed at a voltage peak. Since the transient frequency of the inrush current is much higher than the 60 Hz power frequency, we can assume the instantaneous voltage (V_0) will remain constant over the transient period.

$$I_{peak} = \frac{V_0}{Z_{surge}} \qquad \text{2-5}$$

$$f = \frac{1}{2\pi\sqrt{\left(L_{source}C_1\right)}} \qquad \text{2-6}$$

In this example, the switching surge impedance is determined by the combination of source inductance and the capacitance in a single leg of a bank:

$$Z_{surge} = \sqrt{\frac{L_{source}}{C_1}} \qquad \text{2-7}$$

The instantaneous voltage V_0 is the peak phase voltage across the capacitor when breaker B1 is closed. If the capacitor is initially charged, then this value must be added or subtracted from V_0:

$$V_0 = \sqrt{\frac{2}{3}}\left(V_{rated}\right) = \sqrt{\frac{2}{3}}\left(230k\right) = 187.794kV \qquad \text{2-8}$$

Thus, the expected peak current and frequency of oscillation are:

$$I_{peak} = 3784\,A \qquad f = 851.84\,Hz$$

The inrush current magnitude is approximately 20 times higher than the peak current at the power frequency. This significant increase in current, if too high, can damage the circuit breaker. Therefore, the peak magnitude and frequency of the inrush current must be limited to values specified by breaker standards.[2]

The maximum allowable $\frac{di}{dt}$ for a 40 kA rated breaker (at 60 Hz) is:

$$\frac{di}{dt}_{allow} = \frac{\sqrt{2} \cdot 40k \cdot 2\pi \cdot 60}{10^6} = 21.326\frac{A}{\mu s} \qquad \text{2-9}$$

Thus, it can be readily shown that the minimum source impedance required for this situation, without additional mitigation measures, is about 3.5 Ω (see simplified circuit *cap_bank_study_01_B.pscx* for illustration).

If the observed transients are greater than those allowable for the breaker (i.e. the system impedance is low), additional series reactance may need to be included.

Other mitigation options include:

- Pre-insertion resistors in parallel with the breakers in the capacitor bank:

[2] IEEE C37.06.2000, p. 7.

- The pre-insertion resistance will damp out the transients. Its value can be determined using the following equation:

$$R_{optimum} = \sqrt{\frac{L_{source}}{C_1}} \qquad 2\text{-}10$$

- These resistors must be shorted during normal operations in order to reduce losses.

- Synchronize the closing of breaker poles; energizing a capacitor when its voltage is closest to zero will result in a reduced transient.

Objectives

The main objectives of a capacitor switching study are to demonstrate that:

- The peak switching overvoltage is less than the rated switching surge insulation level of units connected to the capacitor bus.
- The peak switching magnitude and frequency of inrush current is less than the rating of the breaker surge insulation level.

Simulation Results

In this example, the multiple-run component is used to energize the capacitor at different points along the voltage waveform.

The simulation results from the simplified circuit (*cap_bank_study_01_B.pscx*) are displayed in Figure 4. The simulation results show that the inrush current attains a peak value of approximately 3.6 kA at a maximum frequency of approximately 850 Hz. These values are very close to the calculated values listed above in the Analysis section and are within the breaker standard limits.

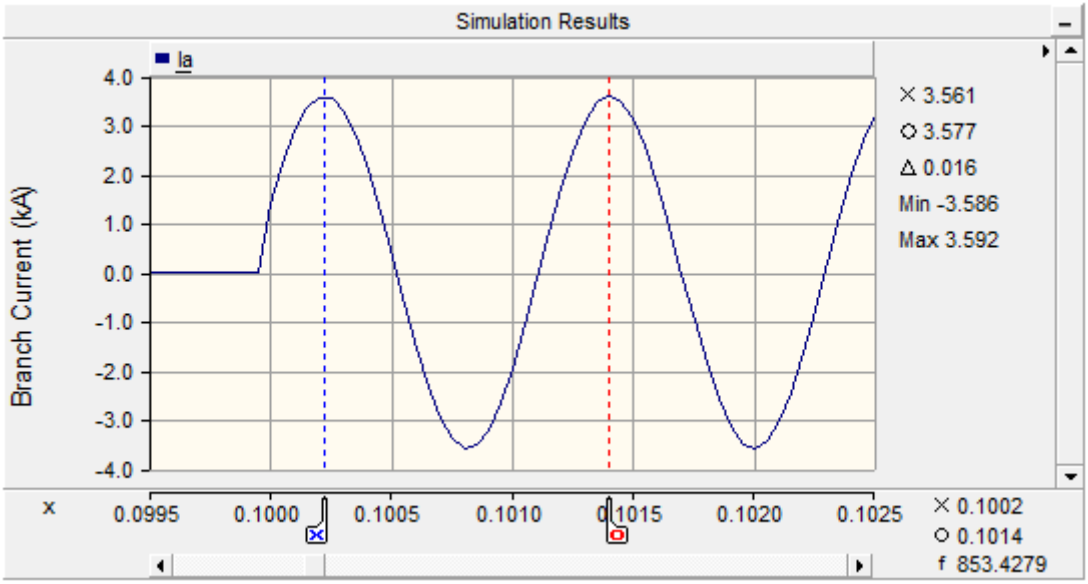


Figure 4: Inrush Current for cap_bank_study_01_B.pscx

The source impedance given in the detailed circuit (*cap_bank_study_01_A.pscx*) is approximately 10 Ω. The simulation results displayed in Figure 5 and Figure 6 demonstrate that the peak and frequency of the transient are much lower in magnitude (approximately 2.0 kA and 500 Hz respectively) than those observed in the simplified circuit (*cap_bank_study_01_B.pscx*). The maximum $\frac{di}{dt}$ is approximately 8.887 A/µs (see Figure 5).

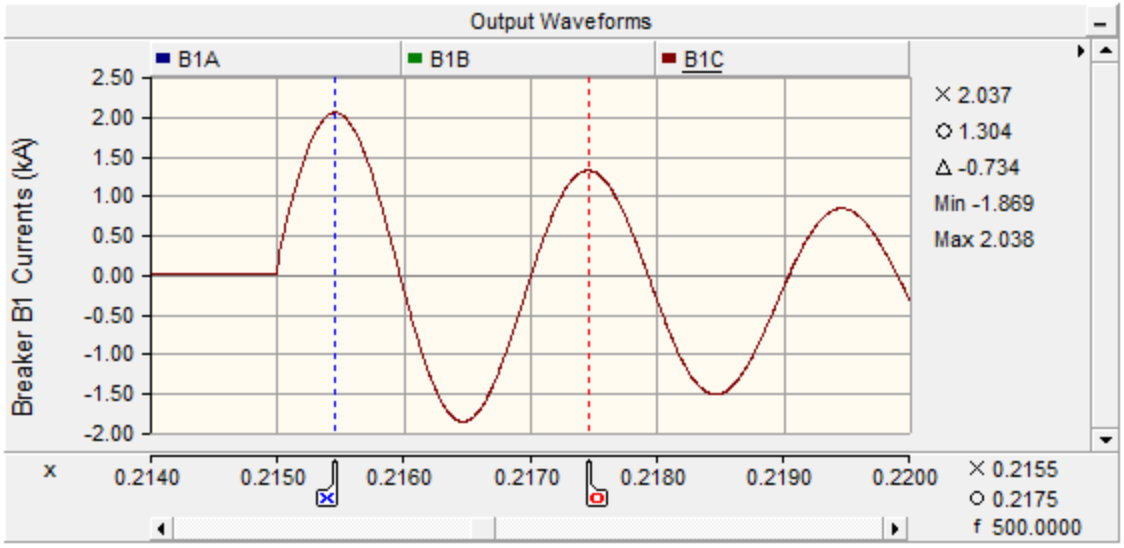


Figure 5: Inrush Current for cap_bank_study_01_A.pscx

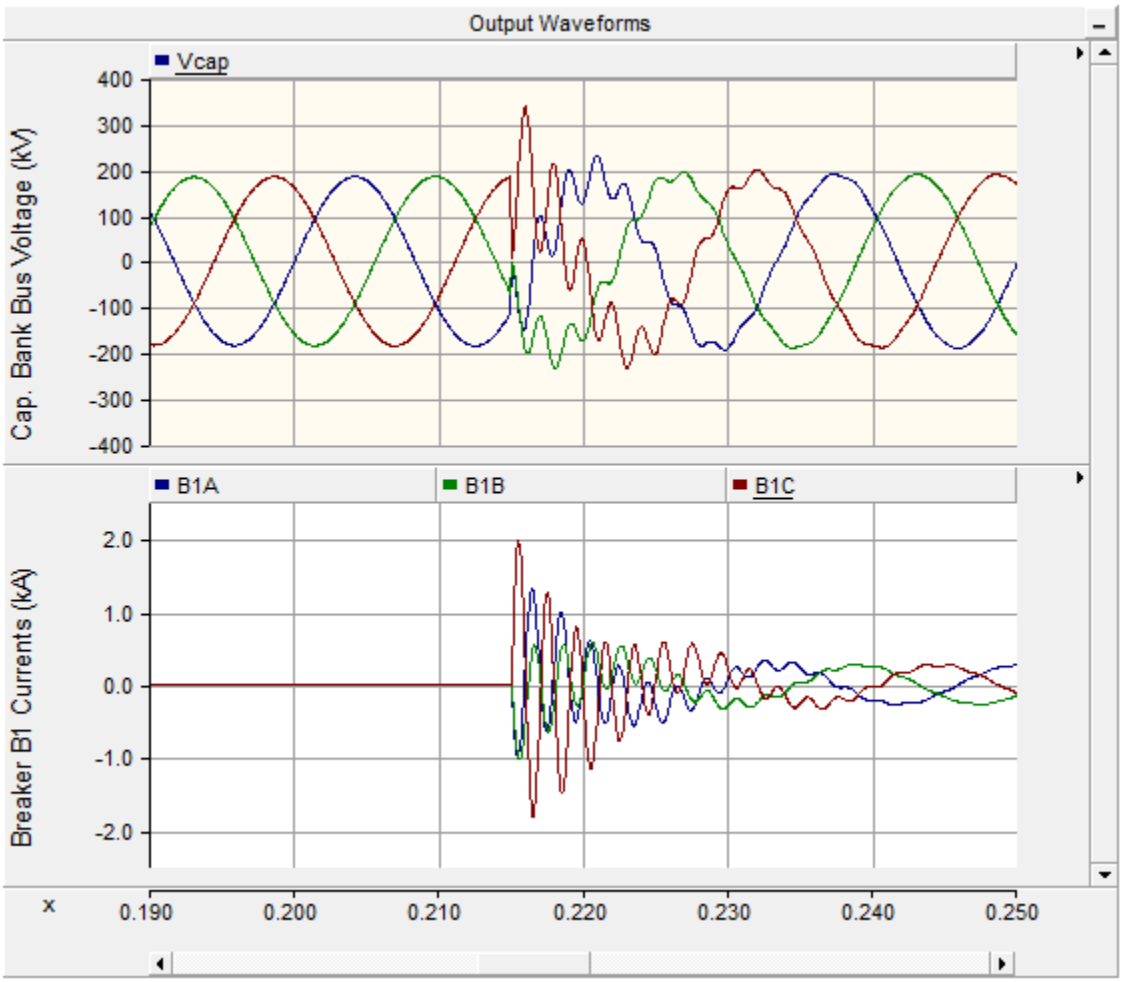


Figure 6: Simulation Results for cap_bank_study_01_A.pscx

Hints

The following are some helpful hints to consider during this study:

- Use the 'Snapshot' feature to speed up the multiple run simulations.
- Disable graphic animation during multiple runs to speed up the simulation.

Discussion

This example considers energizing only a single capacitor. However, the worst case is more likely when energizing a second, third and fourth leg, after the previous have reached steady-state (i.e. back-to-back switching). This is addressed in Section 2.2.

PSCAD

Refer to PSCAD cases: *cap_bank_study_01_A.pscx* and *cap_bank_study_01_B.pscx*

References

1. “Modeling and Analysis of System Transients Using Digital Programs”, IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-13 to 4-14.

2.2 Back-to-Back Capacitor Switching Study: Transient Overvoltage and Inrush Current

Motivation

The purpose of this study is to illustrate key points to be considered in a back-to-back capacitor switching study. After an energized capacitor reaches steady-state, another capacitor in the bank is energized. This leads to an inrush current transient involving the closed-loop containing the two capacitor legs. The magnitude and frequency of the transient current can potentially reach very high values. This is because there is very little reactance in this closed-loop to limit the current. If the transient current is excessive, additional inrush reactors must be installed.

System Overview

The network model and the details for this study are as outlined in Section 2.1. We will be focusing on the PSCAD example project *cap_bank_study_02.pscx*, which is virtually identical to *cap_bank_study_01_A.pscx*.

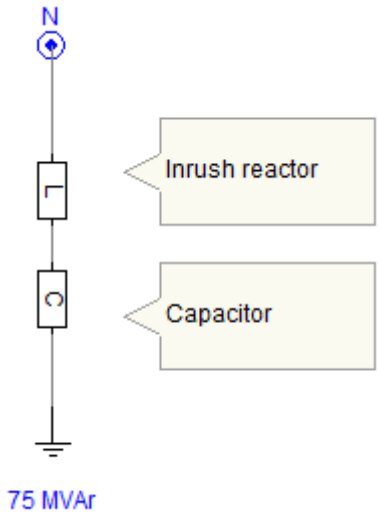


Figure 7: A Single Leg of the 230 kV Capacitor Bank (cap_bank_study_01_A.pscx)

In each situation a single breaker is being energized. One or more of the other capacitor banks are already connected. The transient current will depend on the number of banks already in service and should be considered in the study.

In general, the worst case situation is likely when all other banks are in service and the last bank is being energized.

Analysis

Figure 8 shows an equivalent circuit illustrating a situation where a second capacitor is being energized; following the first reaching steady-state (breakers B3 and B4 remain open). Since the transient current frequency is much greater in magnitude than it is at the power frequency, we can

neglect the impact from the system side for the simplified analysis. Note that $L_{station}$ consists of the internal inductance of the capacitors and the bus inductance between banks. Since its value is negligible, compared to the inrush reactor inductance (L_1 and L_2), it has been omitted from calculations. However, in some cases, $L_{station}$ may be sufficient to limit the inrush transients and additional inrush reactors may not be required.

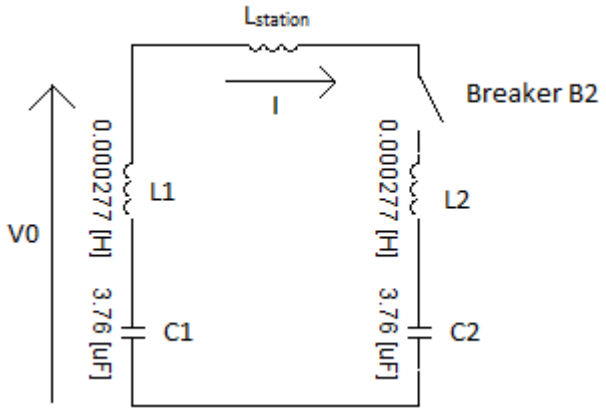


Figure 8: Equivalent Circuit of Back-to-Back Switching

When breaker B2 is closed, capacitor C1 will discharge through the newly energized capacitor C2, creating a large inrush current. To determine the magnitude and frequency of the inrush current, the following equations can be used:

$$I_{peak} = \frac{V_0}{Z_{surge}} \qquad 2\text{-}11$$

$$f = \frac{1}{2\pi\sqrt{(L_{eq} \times C_{eq})}} \qquad 2\text{-}12$$

$$I \times f = \frac{V_0}{2\pi \cdot L_{eq}} \qquad 2\text{-}13$$

Where:

$$Z_{surge} = \sqrt{\frac{L_{eq}}{C_{eq}}}$$

$$L_{eq} = L_1 + L_2$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$V_0 = \sqrt{\frac{2}{3}} V_{rated}$$

- peak phase voltage across capacitors

From the equations listed above we calculate the following:

$$L_{eq} = 0.000277 + 0.000277 = 0.000554 H$$

$$C_{eq} = \frac{3.76\mu \cdot 3.76\mu}{3.76\mu + 3.76\mu} = 1.88\,\mu F$$

$$Z_{surge} = \sqrt{\frac{0.000554}{1.88\mu}} = 17.166\,\Omega$$

$$V_0 = \sqrt{\frac{2}{3}}(230k) = 187.794\,kV$$

Thus, the expected peak current and the frequency of oscillation are:

$$I_{peak} = 10.954\,kA \qquad f = 4925\,Hz$$

The peak magnitude and frequency of the initial inrush current must be limited to values specified by breaker standards.[3] For this example, in which the capacitor bus voltage is rated at 230 kV, the limit is:

$$I_{peak} \times f \;\le I_{peak\_rated} \times f_{rated} = 20\,kA \times 4.25\,kHz = 85 \times 10^6\,AHz$$

An inrush reactor added in series with the capacitor was used to limit the magnitude and frequency of the current to values within this standard. The inrush reactor inductance was estimated using the following equation with the relevant values listed in the breaker standards.[4]

$$L_{eq} = \frac{V_0}{2\Pi\left(I_{peak\_rated} \times f_{rated}\right)} \qquad \text{2-14}$$

$$L_{eq} = \frac{187.794k}{2\Pi\left(85 \times 10^6\right)} = 0.00035\,H$$

[3] IEEE C37.06.2000, p. 7.
[4] IEEE C37.06.2000, p. 7

For this example, the inrush reactor inductance is determined to be as follows since there are four legs in the capacitor bank:

$$L_{eq} = 0.00035H \approx \left(L_1 // L_2 // L_3\right) + L_4$$

$$\therefore L_1 = L_2 = L_3 = L_4 = 0.000277H$$

Objective

The main objective of a capacitor switching study is to demonstrate that the peak switching magnitude and frequency of inrush current is less than the rating of the breaker.

Simulation Results

In this example, the PSCAD multiple-run component is used to energize the capacitor at different points along the voltage waveform. The multiple-run is set up to repeat the simulation approximately 20 times. On each run, the breaker closes at a different point on the voltage waveform.

Scenario 1

In this scenario, the second leg in the capacitor bank is energized. Breaker B1 is initially closed, breaker B2 is closed to energize the second leg, and breakers B3 and B4 are left open.

The simulation results displayed in Figure 9 and Figure 10 are for the worst case situation, in which the inrush current attains a peak value of approximately 10.1 kA and a maximum frequency of Hz. The simulations follow the hand calculations in the Analysis section closely and these values are within the limits set by the breaker standards. Note that the inrush current is much greater in magnitude than it is in Section 2.1, where only the first capacitor leg was energized. The greater magnitude occurs here because we have a very small local impedance path for the current, under the back-to-back switching condition.

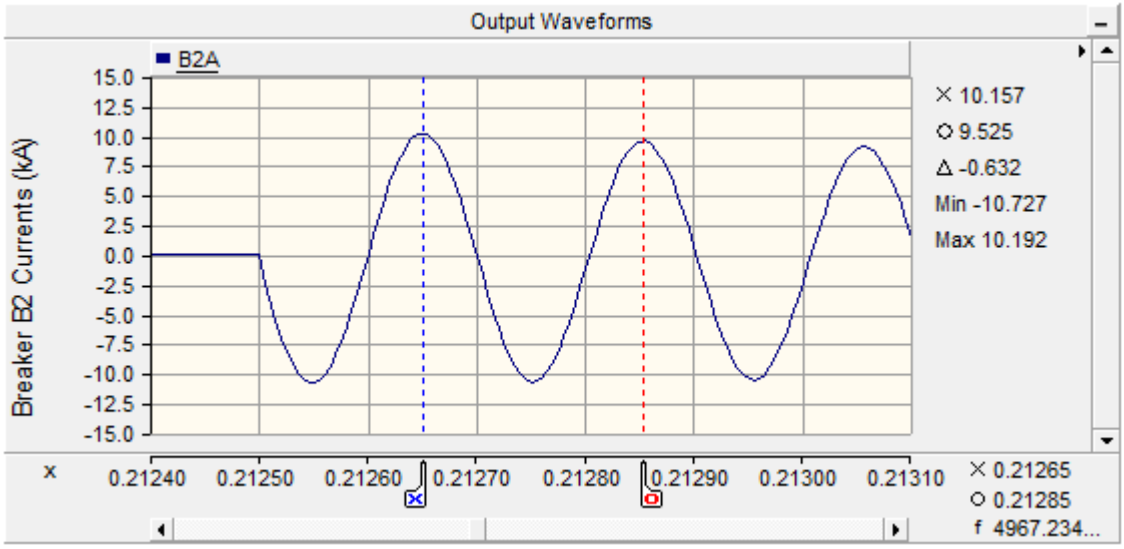


Figure 9: Maximum Inrush Current Magnitude and Frequency

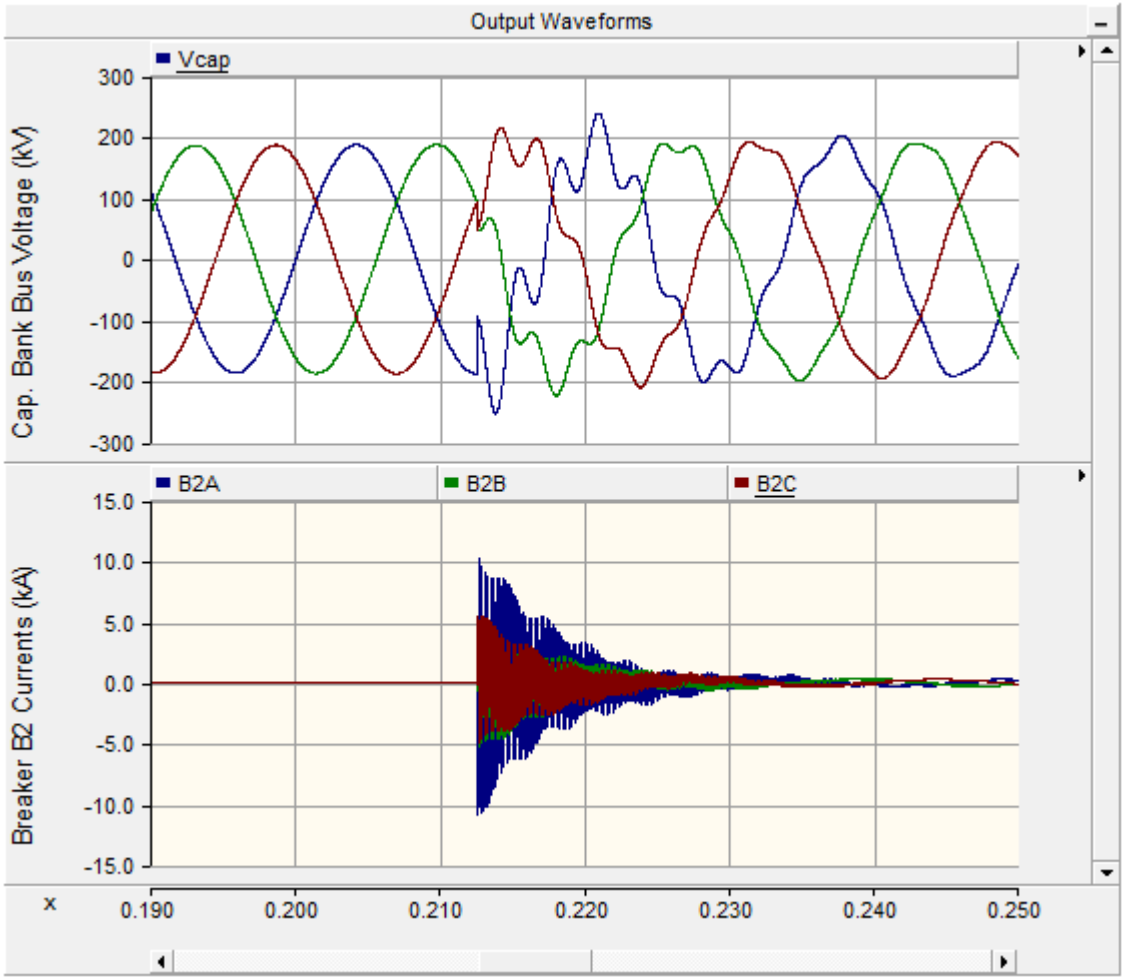


Figure 10: Simulation Results for Energizing the Second Capacitor

Scenario 2

In this scenario, the third leg in the capacitor bank is energized. Breakers B1 and B2 are initially closed; breaker B3 is closed to energize the third bank, and breaker B4 is left open, as demonstrated by:

$$L_{eq} = L_3 + \frac{L_1 \cdot L_2}{L_1 + L_2} = 0.000277 + \frac{0.000277 \cdot 0.000277}{0.000277 + 0.000277} = 0.0004155H$$

$$C_{eq} = \frac{2C \cdot C}{2C + C} = \frac{(2 \times 3.76\mu) \cdot 3.76\mu}{(2 \times 3.76\mu) + 3.76\mu} = 2.513\mu F$$

Using Equations 2-11 and 2-12 from the Analysis section, we find the expected magnitude and frequency of the inrush current to be:

$$I_{peak} = 14.606kA \qquad f = 4925Hz$$

The simulation results for this worst case situation show the inrush current attains a peak value of approximately 14.8 kA and a maximum frequency of 4.9 kHz. The simulation results follow the hand calculations closely and these values are within the limits set by the breaker standards.

Scenario 3

In this scenario, the fourth leg in the capacitor bank is energized. Breakers B1, B2 and B3 are initially closed, and breaker B4 is closed to energize the fourth leg. This is demonstrated by:

$$L_{eq} = L_4 + L_1 // L_2 // L_3 = 0.0003693H$$

$$C_{eq} = \frac{3C \cdot C}{3C + C} = \frac{(3 \times 3.76\mu) \cdot 3.76\mu}{(3 \times 3.76\mu) + 3.76\mu} = 2.82\mu F$$

Using Equations 2-11 and 2-12 from the Analysis section, we find the expected magnitude and frequency of the inrush current to be:

$$I_{peak} = 16.431kA \qquad f = 4925Hz$$

The simulation results for the worst case situation show the inrush current attains a peak value of approximately 16.8 kA and a maximum frequency of 4.9 kHz. The simulation follows the hand calculations closely and these values are within the limits set by the breaker standards.

Discussion

Energizing each leg in the capacitor bank individually will gradually increase the inrush current until it reaches its maximum value, which occurs when all capacitors are energized. Energizing the bank in this way will help prevent damage to devices connected to the capacitor bank bus. Also, reactors will limit the inrush current magnitude and frequency, so as to conform to breaker standards and are the recommended mitigation method in capacitor bank applications.

PSCAD

Refer to PSCAD case: *cap_bank_study_02.pscx*

Additional Notes

Once the initial transient has had time to settle, a common voltage across the two capacitors will be reached (according to the conservation of charge). Figure 11 represents the equivalent circuit at this point.

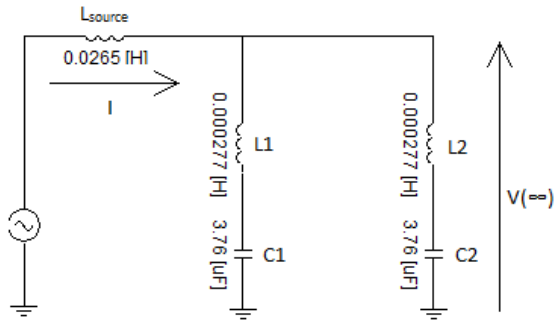


Figure 11: Equivalent Circuit when Common Voltage is Reached

The common voltage across the capacitors V(∞), when the initial charge on the second capacitor C2 is zero, is determined to be 93.9 kV:

$$C_1 V_{C1}(0) + C_2 V_{C2}(0) = (C_1 + C_2) V(\infty)$$

$$V(\infty) = \frac{C_1 V_{C1}(0) + C_2 V_{C2}(0)}{(C_1 + C_2)} = \frac{(3.76\mu \times 87.794k) + (3.76\mu \times 0)}{(3.76\mu + 3.76\mu)} = 93.9kV$$

Since V(∞) is less than the system voltage, a current will be drawn into the capacitor banks, creating a second transient. However, the magnitude and frequency of the inrush current is not as large as the initial transients, because the voltage across the capacitors has been reduced and the surge impedance has increased. This is demonstrated by:

$$L_{eq} = L_{source} + \frac{L_1 \cdot L_2}{L_1 + L_2} = 0.0264 + \frac{0.000277 \cdot 0.000277}{0.000277 + 0.000277} = 0.02664\,H$$

$$C_{eq} = C_1 + C_2 = 7.52\mu F$$

$$I_{peak} = \frac{V_{source} - V(\infty)}{Z_{surge}} = \frac{(187.794k - 93.9k)}{59.52} = 1.57kA$$

$$f = \frac{1}{(2\Pi\sqrt{L_{eq} C_{eq}})} = \frac{1}{(2\Pi\sqrt{7.52\mu \cdot 0.02664})} = 355.59Hz$$

Therefore, in back-to-back capacitor switching, there are two inrush currents that are produced: The first is created from the already energized capacitor discharging into the newly switched capacitor. The second transient is produced when the two capacitors reach a common voltage that is lower than the system voltage, leading to a current being drawn into the parallel capacitor banks.

References

1. “Modeling and Analysis of System Transients Using Digital Programs”, IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-15.

2.3 Capacitor Bank Discharge and Transient Outrush Currents Study

Motivation

The purpose of this study is to illustrate key points to be considered when a capacitor bank discharges into a nearby fault, resulting in the production of transient outrush currents. The frequency, peak, and rate of change (i.e. $\frac{di}{dt}$) of the current must be controlled in order to ensure that the circuit breaker can withstand the capacitor outrush current without sustaining damage.

System Overview

The network model and the details for this study are similar to those outlined in Section 2.1. However, an outrush reactor has been added to the circuit, as shown in Figure 12.

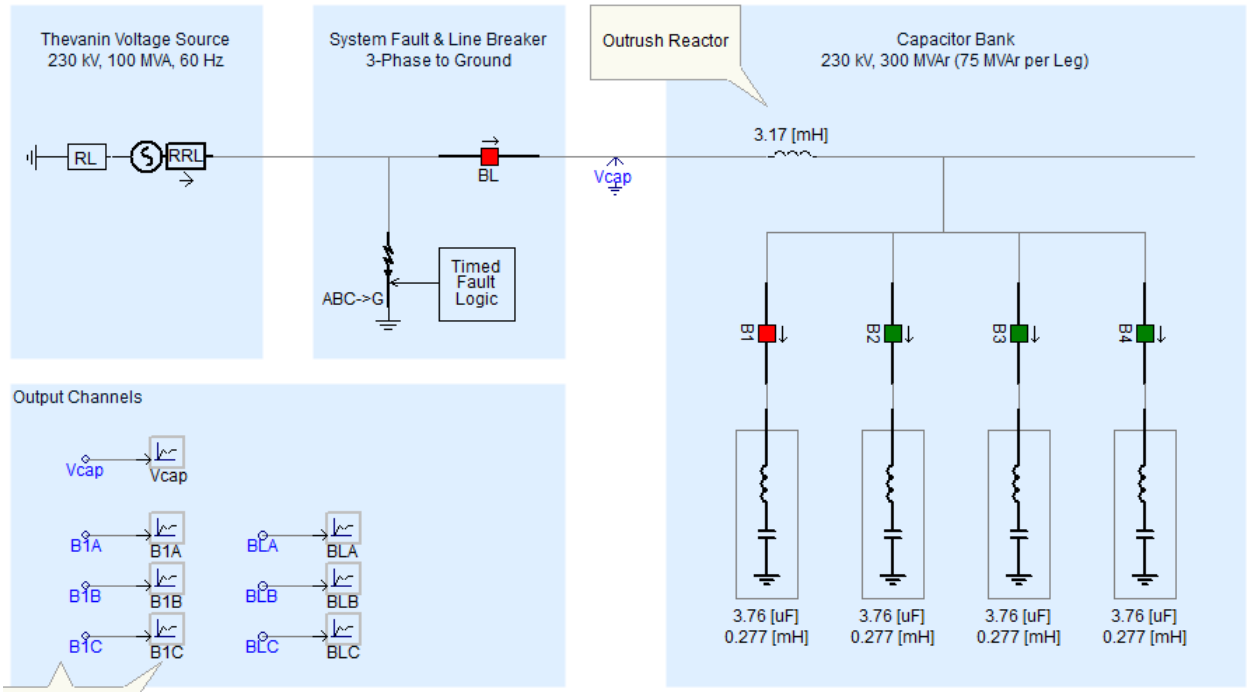


Figure 12: The 230 kV Capacitor Bank (First Capacitor Energized)

A fault in the system, occurring very close to the capacitor bank, is considered for the purpose of determining the outrush reactor requirements. In this situation, the capacitors will discharge through the faulted path. The severity of the transient current will be limited by the reactance in this path. The function of the outrush reactor is to limit this discharge current.

The transients also depend on the number of banks in service at the time of the fault. However in general, the worst case situation is likely when all banks are in service.

Analysis

Figure 13 illustrates an equivalent circuit diagram for a situation in which a single leg of a capacitor bank is in operation at the time of the fault.

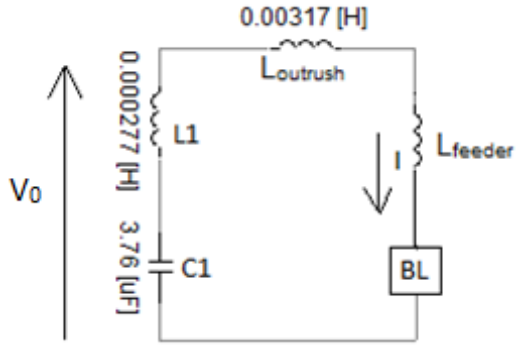


Figure 13: Equivalent Circuit Demonstrating Outrush Current

Following the occurrence of a nearby fault on the capacitor bus, the capacitor C1 will discharge to the fault through the breaker BL, creating a large outrush current. The closer the fault is to the bus, the larger the outrush current will be, due to the dependence on feeder inductance L_{feeder}, which decreases with proximity. In this example, the fault occurs at the bus to simulate the worst case situation (i.e. $L_{feeder}= 0$). To determine the magnitude and frequency of the outrush current; the following equations can be used:

$$I_{peak} = \frac{V_0}{Z_{surge}} \qquad 2\text{-}15$$

$$f = \frac{1}{2\pi\sqrt{(L_{eq} \times C_{eq})}} \qquad 2\text{-}16$$

Where:

$$Z_{surge} = \sqrt{\frac{L_{eq}}{C_{eq}}}$$

$$L_{eq} = L_1 + L_{outrush} + L_{feeder}$$

$$C_{eq} = C_1$$

$$V_0 = \sqrt{\frac{2}{3}} V_{rated}$$

- peak phase voltage across capacitors

From the equations listed above, we find the following results:

$$L_{eq} = 0.000277 + 0.00317 + 0 = 0.003447\,H$$

$$C_{eq} = 3.76\,\mu F$$

$$Z_{surge} = \sqrt{\frac{0.003447}{3.76\mu}} = 30.28\Omega$$

$$V_0 = \sqrt{\frac{2}{3}}(230k) = 187.794\,kV$$

Thus, the expected peak current and frequency of oscillation are:

$$I_{peak} = 6.201kA \qquad f = 1398\,Hz$$

The product of the peak magnitude and the maximum frequency of the outrush current must be limited to values less than 2x10^7, as specified by IEEE standards.[5] Also, the current-frequency rating is dependent only on the inductance of the equivalent circuit. This is demonstrated by:

$$I \times f = \frac{V_0}{2\pi(Leq)} \qquad \text{2-17}$$

Therefore, increasing the equivalent inductance will reduce the value of $I \times f$ so that it falls within breaker standards. In this example, a current limiting outrush reactor, added in series with the capacitor bank, is used to limit the value of current magnitude and frequency. The reactor also increases the surge impedance, thereby reducing the inrush current. The outrush reactor inductance can be estimated using the following equation:

$$L_{eq} \geq \frac{V_0}{2\pi(I \times f)} \quad \text{where: } (I \times f) = 2 \times 10^7 \qquad \text{2-18}$$

Accordingly, an outrush reactor whose inductance is greater than about 0.0015 H will be sufficient to limit the transients to acceptable levels (case *cap_bank_study_03.pscx* uses an outrush reactor of 0.00317 H, which is more than the minimum requirement).

[5] IEEE C37.06.2000, p. 9

Objective

The main objective of a capacitor bank discharge study is to demonstrate that the peak switching magnitude and frequency of outrush current is less than the ratings of the breaker.

Simulation Results

In this example, the PSCAD multiple-run component is used to create a fault at different points along the voltage waveform. The multiple-run is set up to repeat the simulation approximately 20 times. On each run, the fault occurs at a different point on the voltage waveform.

Scenario 1

The first capacitor bank is discharged. Breaker B1 is initially closed, and breakers B2, B3 and B4 are left open.

The simulation results shown in Figure 14 and Figure 15 are for the worst case, where the outrush current attains a peak value of approximately 6.2 kA and a maximum frequency of 1.4 kHz. The simulation follows closely the hand calculations from the Analysis section, and these values are within the limits set by the breaker standards. This is demonstrated by:

$$I_{peak} \times f = 6.19k \times 1.40k = 0.8668 \times 10^7 < 2 \times 10^7$$

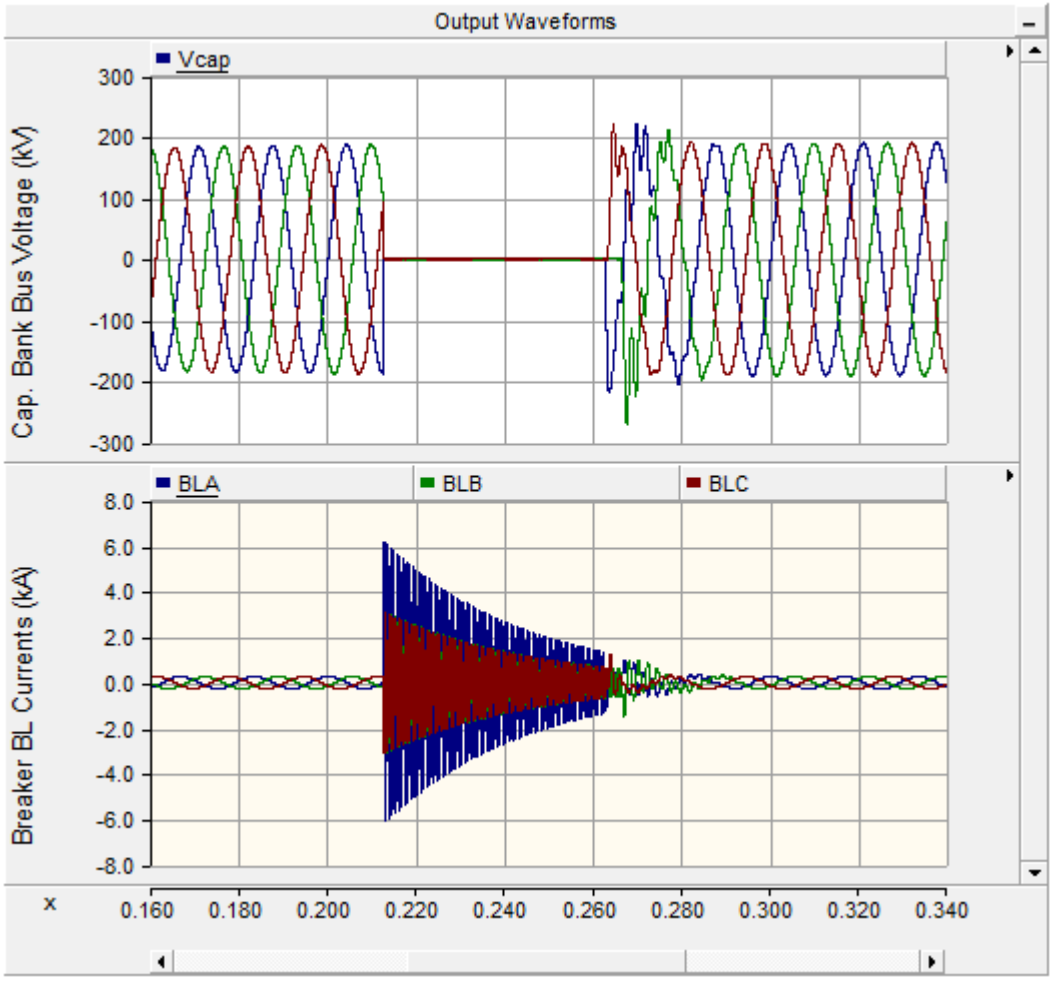


Figure 14: Simulation Results from Discharging a Single Capacitor through Breaker BL

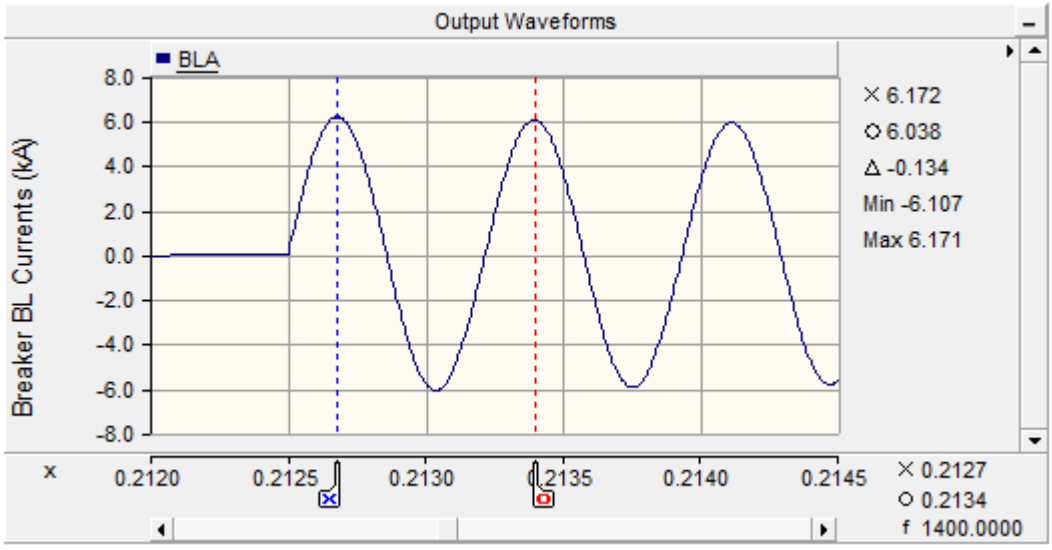


Figure 15: Maximum Outrush Current through Breaker BL (Phase A)

Scenario 2

Two legs of the capacitor bank are discharged. Breakers B1 and B2 are initially closed and breakers B3 and B4 are left open, as demonstrated by:

$$L_1 = L_2 = 0.000277\,H$$

$$L_{eq} = L_{outrush} + \frac{L_1 \cdot L_2}{L_1 + L_2} = 0.003309\,H$$

$$C_{eq} = 2C = 7.54\,\mu F$$

Using equations 2-15 and 2-16 from the Analysis section, we find the expected magnitude and frequency of the outrush current to be:

$$I_{peak} = 8.965\,kA \qquad f = 1008\,Hz$$

The simulation results for the worst case situation show the outrush current attains a peak value of approximately 9.0 kA and a maximum frequency of 1.0 kHz. The simulation follows the hand calculations closely, and these values are within the limits set by the breaker standards.

Scenario 3

Three legs of the capacitor bank are discharged. Breakers B1, B2 and B3 are initially closed, and breaker B4 is open. This is represented by:

$$L_1 = L_2 = L_3 = 0.000277\ H$$

$$L_{eq} = L_{outrush} + L_1 // L_2 // L_3 = 0.003262\,H$$

$$C_{eq} = 3C = 11.31\,\mu F$$

Using equations 2-15 and 2-16 from the Analysis section, we find the expected magnitude and frequency of the inrush current to be:

$$I_{peak} = 11.057\,kA \qquad f = 825.561\,Hz$$

The simulation results for the worst case show the inrush current attains a peak value of approximately 11.4 kA and a maximum frequency of 831Hz. The simulation follows the hand calculations closely, and these values are within the limits set by the breaker standards.

Scenario 4

All four legs of the capacitor bank are discharged. Breakers B1, B2, B3 and B4 are initially closed. This is represented by:

$$L_1 = L_2 = L_3 = L_4 = 0.000277\,H$$

$$L_{eq} = L_{outrush} + L_1 // L_2 // L_3 // L_4 = 0.003239\,H$$

$$C_{eq} = 3C = 11.31\,\mu F$$

Using equations 2-15 and 2-16 from the Analysis section, we find the expected magnitude and frequency of the inrush current to be:

$$I_{peak} = 12.813\,kA \qquad f = 720.107\,Hz$$

The simulation results for the worst case situation show the inrush current attains a peak value of approximately 13.4 kA and a maximum frequency of 718Hz. The simulations follow the hand calculations closely and these values are within the limits set by the breaker standards.

Discussion

The worst case situation occurs when all four capacitors are in service at the time of the fault.

PSCAD

Refer to case: *cap_bank_study_03.pscx*

References

1. “Modeling and Analysis of System Transients Using Digital Programs”, IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-16.

2.4 Voltage Magnification due to Capacitor Switching Transients Study

Motivation

The purpose of this study is to illustrate a voltage magnification problem that can occur when a large capacitor is energized at a high voltage level, while an existing low-voltage capacitor bank is already energized. This situation can lead to magnification of the voltage transients at the lower voltage capacitor bank. Magnification occurs because energizing the high-voltage capacitor excites a resonant oscillation in the low-voltage capacitor bank, creating severe and sustained transients.

System Overview

A Thévanin equivalent voltage source, representing an 11 kV system, is connected to a 100 kVA, 11/0.415 kV transformer and a 912 kVAr capacitor bank (20 µF). Also connected to the transformer is a 20.8 kVAr capacitor bank (320 µF) at 415 V (i.e. a low voltage industrial power factor correction unit).

The voltage at the low-voltage bus *Eas* is the focus of the study (see Figure 16).

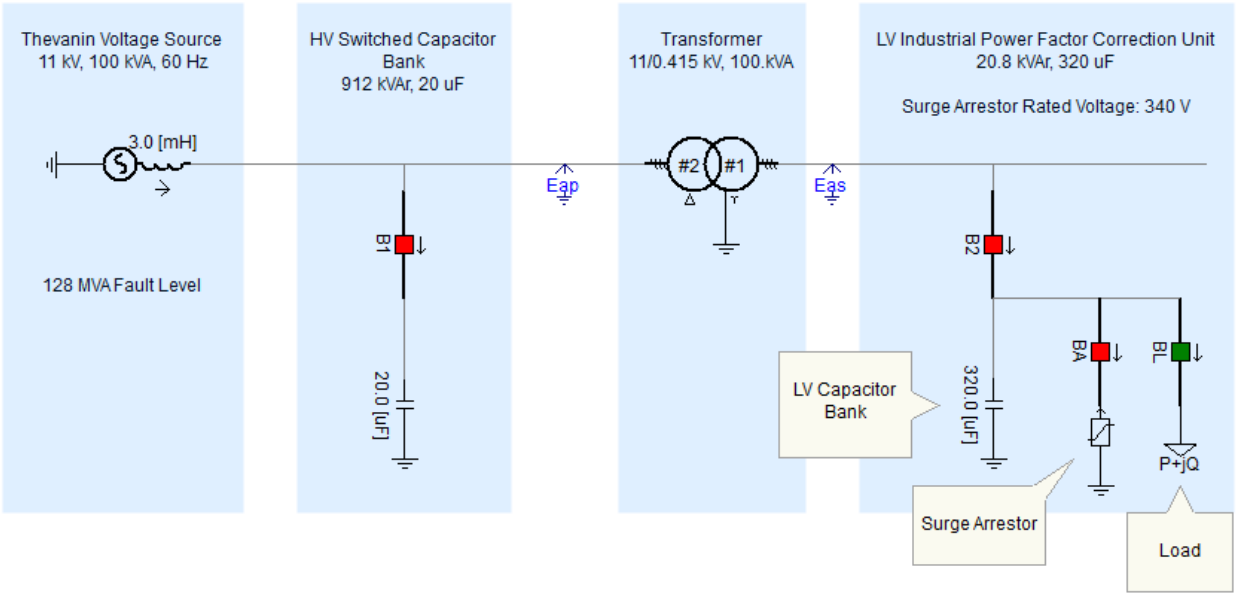


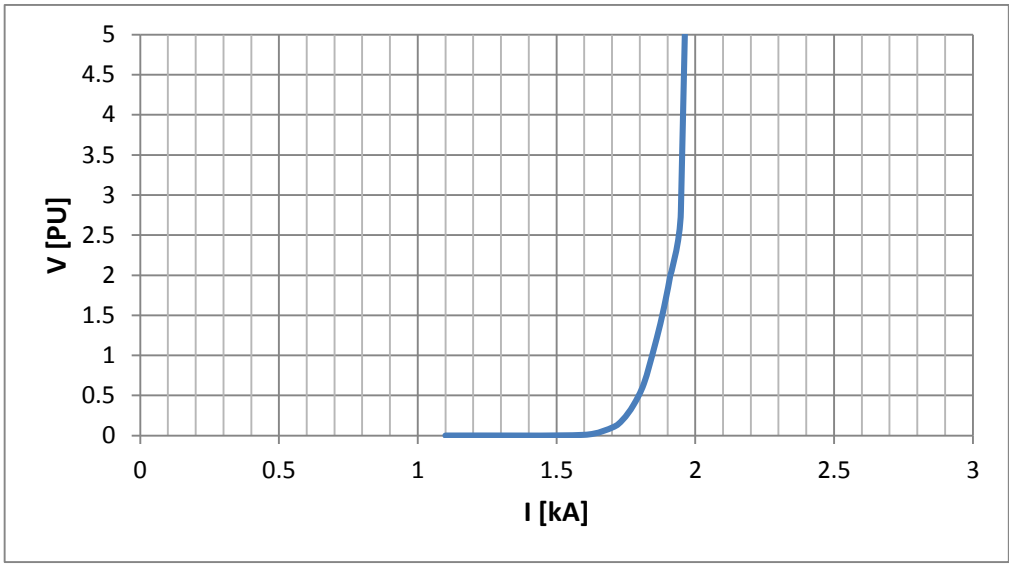
Figure 16: An 11 kV System Connected to a High and Low Voltage Capacitor Bank

Surge Arrestor

Surge arrestors can limit a transient overvoltage from reaching excessive levels. The rated voltage of the surge arrestor (connected from line to ground) in this example is 340 V. The surge arrestor characteristics are listed in Table 1, in which the per-unit voltage is based on the surge arrestor rated voltage.

Table 1: Surge Arrestor Data

V [PU]	I [kA]
1.1	0.001
1.6	0.01
1.7	0.1
1.739	0.2
1.777	0.38
1.815	0.65
1.853	1.11
1.881	1.5
1.91	2
1.948	2.8
3.2	200



Magnification of voltage and current transients will occur when the following conditions exist:

- The kVAr rating of the switched capacitor bank is significantly greater (x10) than the lower voltage capacitor bank.
- The natural frequencies f_1 and f_2 are approximately equal (see a simplified circuit to find natural frequencies in Figure 17).
- There is little damping on the low-voltage (LV) side of the transformer (low loss /lightly loaded).

Figure 17 shows a simplified diagram of the circuit from Figure 16.

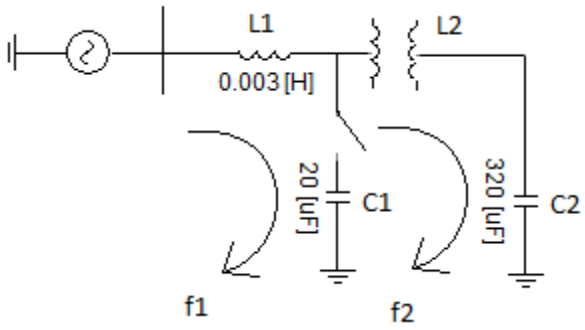


Figure 17: Simplified Circuit to Find Natural Frequencies

The natural frequencies f_1 and f_2 are:

$$f_1 = \frac{1}{\left(2\pi\sqrt{L_1 C_1}\right)}$$ Where: L_1 = source inductance, C_1 = higher voltage capacitance

$$f_2 = \frac{1}{\left(2\pi\sqrt{L_2 C_2}\right)}$$ Where: L_2 = transformer inductance, C_2 = low voltage capacitance

For this case, the natural frequencies are determined to be 649.75 Hz and 658.16 Hz respectively. These values are very close and therefore, transient voltage and current magnification should be a concern.

The transient voltages on the LV side can reach dangerous levels, which can deteriorate the condition of equipment connected to the bus. Therefore, mitigation methods must be investigated.

General mitigation methods to reduce the magnified transient voltages and currents are as follows:

- Synchronized closing of the breakers; energizing a capacitor when its voltage is closest to zero will result in a reduced transient.
- Pre-insertion of the resistors/inductors on the switching capacitor bank(s).
- Moderate increases to the system loading on the LV side of the transformer, which will help to dampen the transient voltages.

The main objectives of a capacitor switching causing transient magnification study are:

- The transient overvoltage is well damped and the magnitudes do not violate the capabilities of transformer and equipment.
- The peak magnified transient voltage is less than the ratings of the transformer insulation levels.
- The energy dissipation in the surge arrestor during the switching surge is within the surge arrestor energy rating.
- Industrial loads are not tripped due to the high frequency transients (i.e. if the load consists of power electronic based industrial drives).

Simulation Results

In this example, the PSCAD multiple-run component is used to energize the HV capacitor bank at different points along the voltage waveform. The multiple-run is set up to repeat the simulation approximately 20 times. On each run, the breaker closes at a different point on the voltage waveform.

Scenario 1

Only the low-voltage capacitor bank is connected to the bus on the LV side of the transformer. The surge arrestor and static load is disconnected in order to observe the theoretical response.

The simulation results shown in Figure 18 are for the worst case situation, where the voltage (Eas) on the LV-side of the transformer, reaches a maximum value of 1.4 kV (4.0 pu). In practice, the surge arrestor will arrest this voltage to a certain extent.

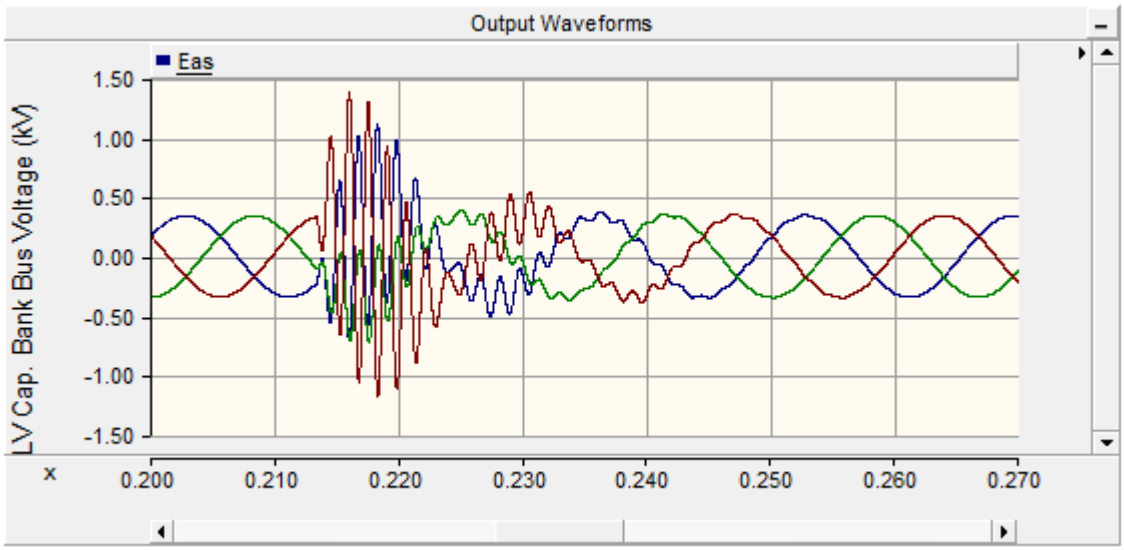


Figure 18: Simulation Results with the LV Capacitor Bank Connected Only

Scenario 2

The capacitor bank and a fixed load are connected to the transformer LV-side bus. The surge arrestor is disconnected in this scenario.

The simulation results shown in Figure 19 are for the worst case situation, where the voltage (Eas) on the LV-side of the transformer reaches a maximum value of 780 V (1.87 pu). Note that the voltage has been reduced significantly. The transient voltage can be reduced further by increasing the resistive load. This simulation illustrates the damping effect of this type of load.

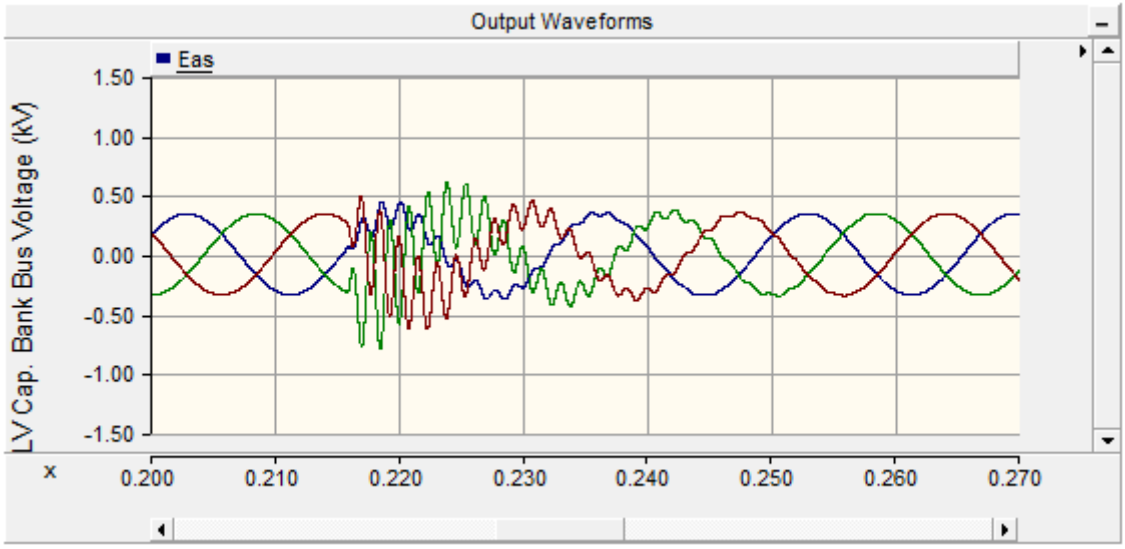


Figure 19: Simulation Results with the LV Capacitor Bank and Fixed Load

Scenario 3

The capacitor bank and the surge arrestor are connected to the transformer LV-side bus. Breaker BL is open, disconnecting the static load.

The simulation results shown in Figure 20 are for the worst case situation when the voltage (Eas) on the LV-side of the transformer reaches a maximum value of 700 V (1.9 pu). In comparing the results between Scenario 1 and Scenario 3, note that the presence of the surge arrestor in Scenario 3 helped to limit the voltage transient.

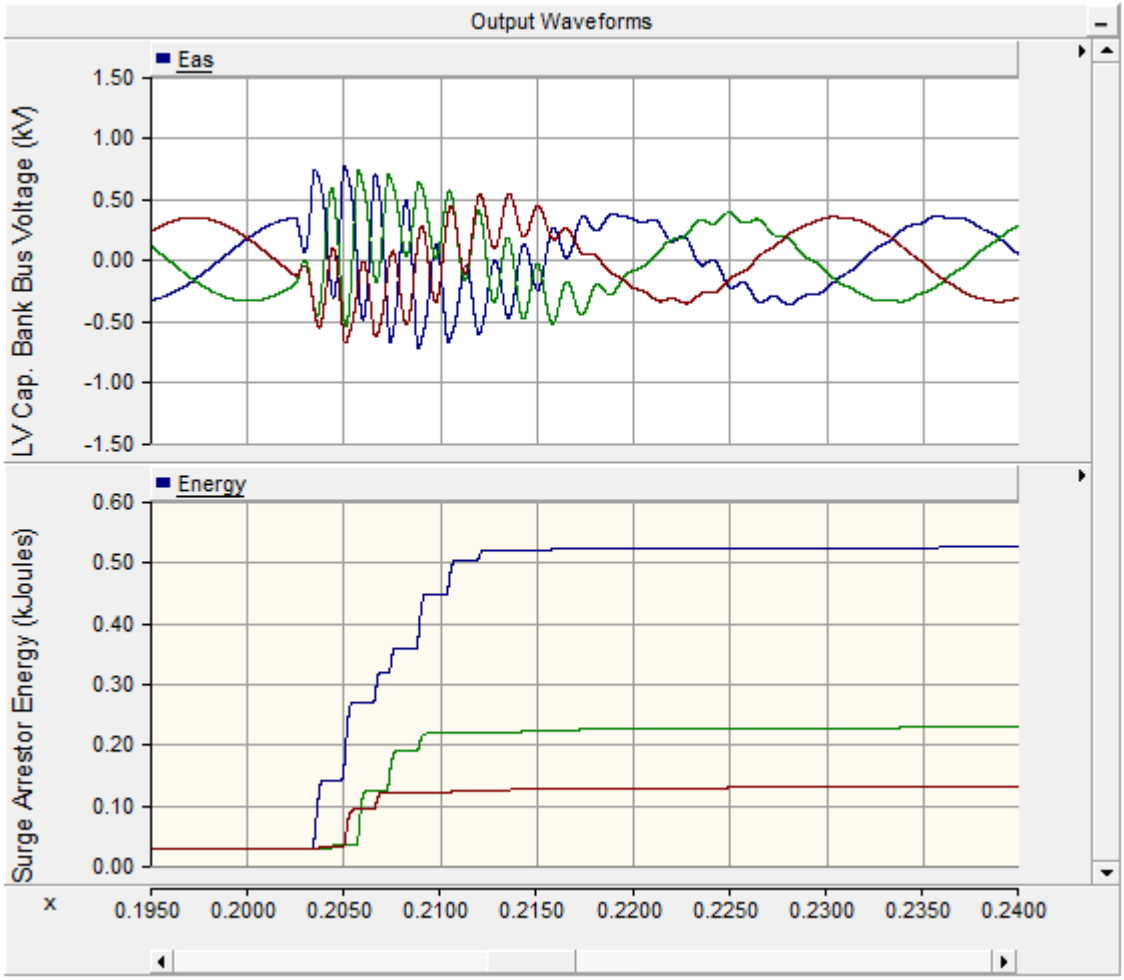


Figure 20: Simulation Results with Surge Arrestor Included

Scenario 4

Only the capacitor on the transformer HV-side is connected. The surge arrestor/load is not present, and the transformer LV-side capacitor is disconnected.

The simulation results shown in Figure 21 are for the worst case situation, where the voltage (Eas) on the LV-side of the transformer reaches a maximum value of 600 V (1.85 pu). The transients have been reduced compared to Scenario 1.

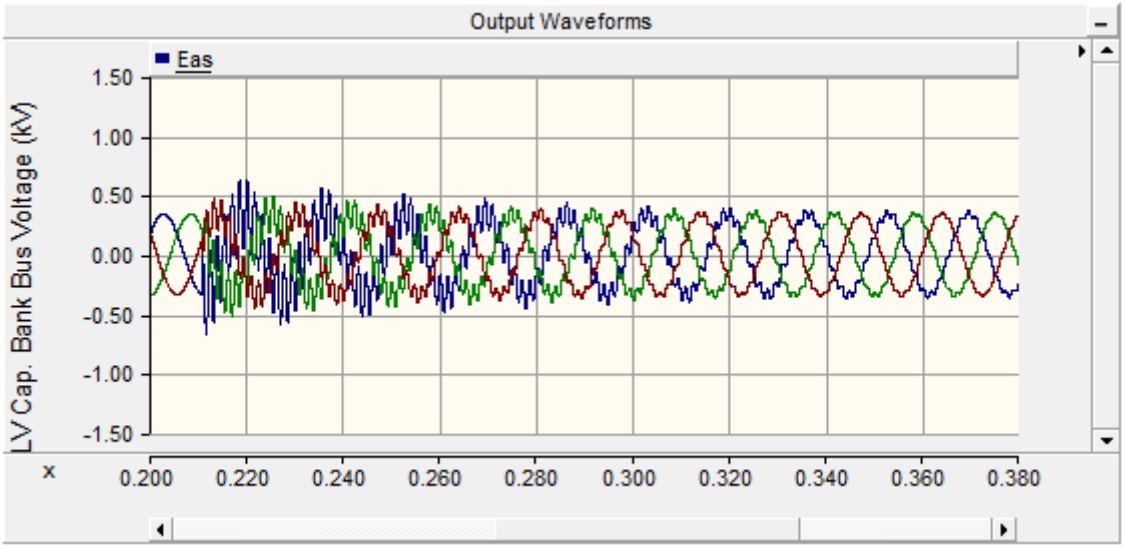


Figure 21: Only the HV Capacitor is Connected to the System

Discussion

The voltage and current amplification problem due to capacitor switching was discussed. Mitigation methods were highlighted.

PSCAD

Refer to case: *cap_bank_study_04.pscx*

References

1. "Modeling and Analysis of System Transients Using Digital Programs", IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-14.

2.5 Breaker Pole Restrike Phenomena within a Capacitor Bank Study

Motivation

The purpose of this study is to illustrate the key points to be considered when the re-energizing of a capacitor bank occurs due to a breaker pole restrike. Restrike occurs when the voltage across the breaker exceeds the dielectric strength of the switch during a switch open operation. This creates very large inrush currents and transient overvoltage.

System Overview

The network model and details are similar to those in Section 2.1. A surge arrestor has been added to the circuit as shown in Figure 22.

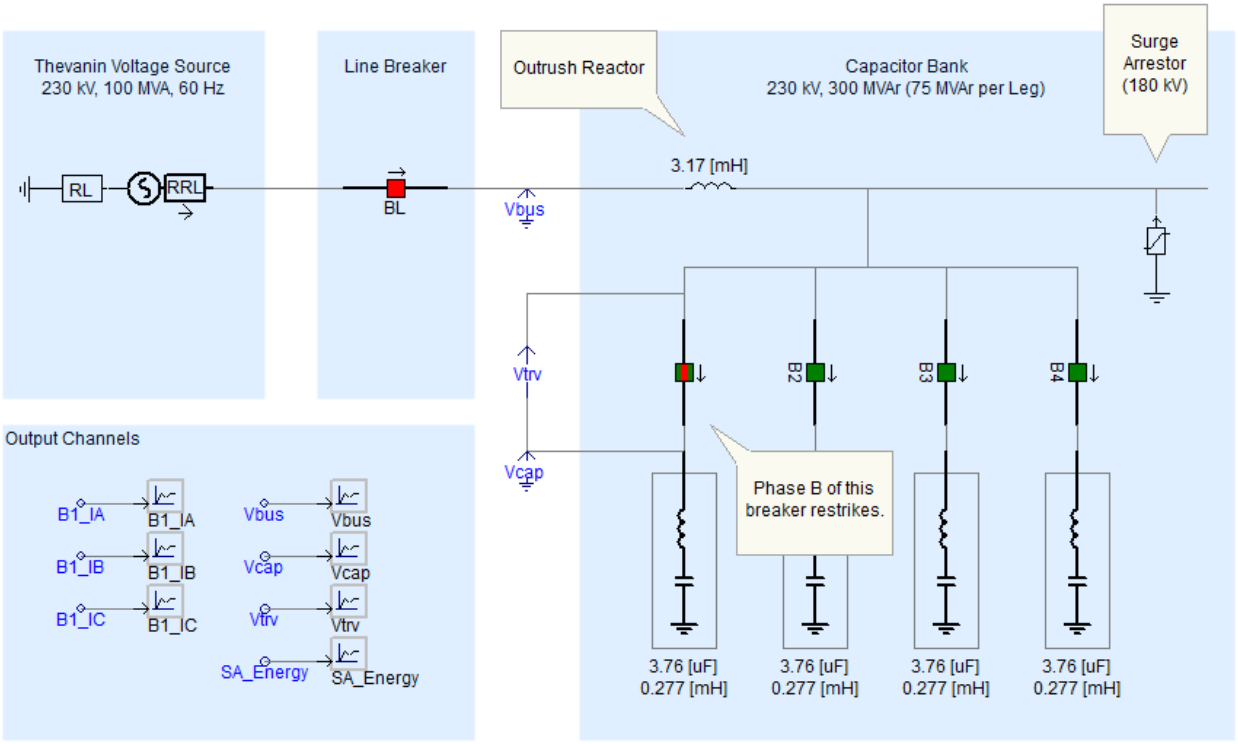


Figure 22: The 230 kV Capacitor Bank with Surge Arrestor

Surge Arrestor

The rated voltage of the surge arrestor (connected from line to ground) in this example is 180 kV, which is typical for a 230 kV system. The surge arrester characteristics are similar to those found in Section 2.4.

Analysis

Figure 23 shows an equivalent circuit for a case in which the first capacitor leg (C1) has been energized and has reached a steady-state (breakers B2, B3 and B4 remain open). At a specified time, breaker B1 will open, interrupting the current flow through the capacitor. After half a cycle, restrike occurs, causing phase B of breaker B1 to reclose when the system voltage is close to the peak value.

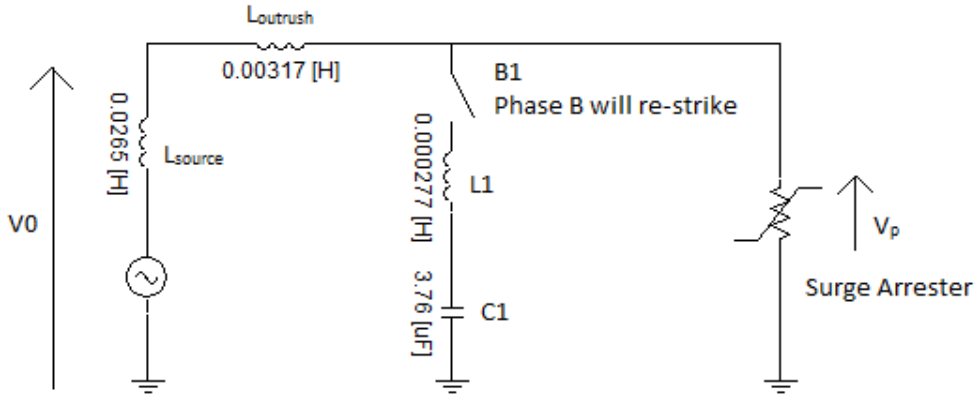


Figure 23: Equivalent Circuit when C1 is Initially Energized Prior to Restrike

When the current through a capacitor is interrupted at a current zero, the capacitor will hold the voltage at which it was interrupted. In a capacitive element, the current leads the voltage by 90°. Therefore, the voltage will be at a maximum when the current is interrupted. This is demonstrated in Figure 24.

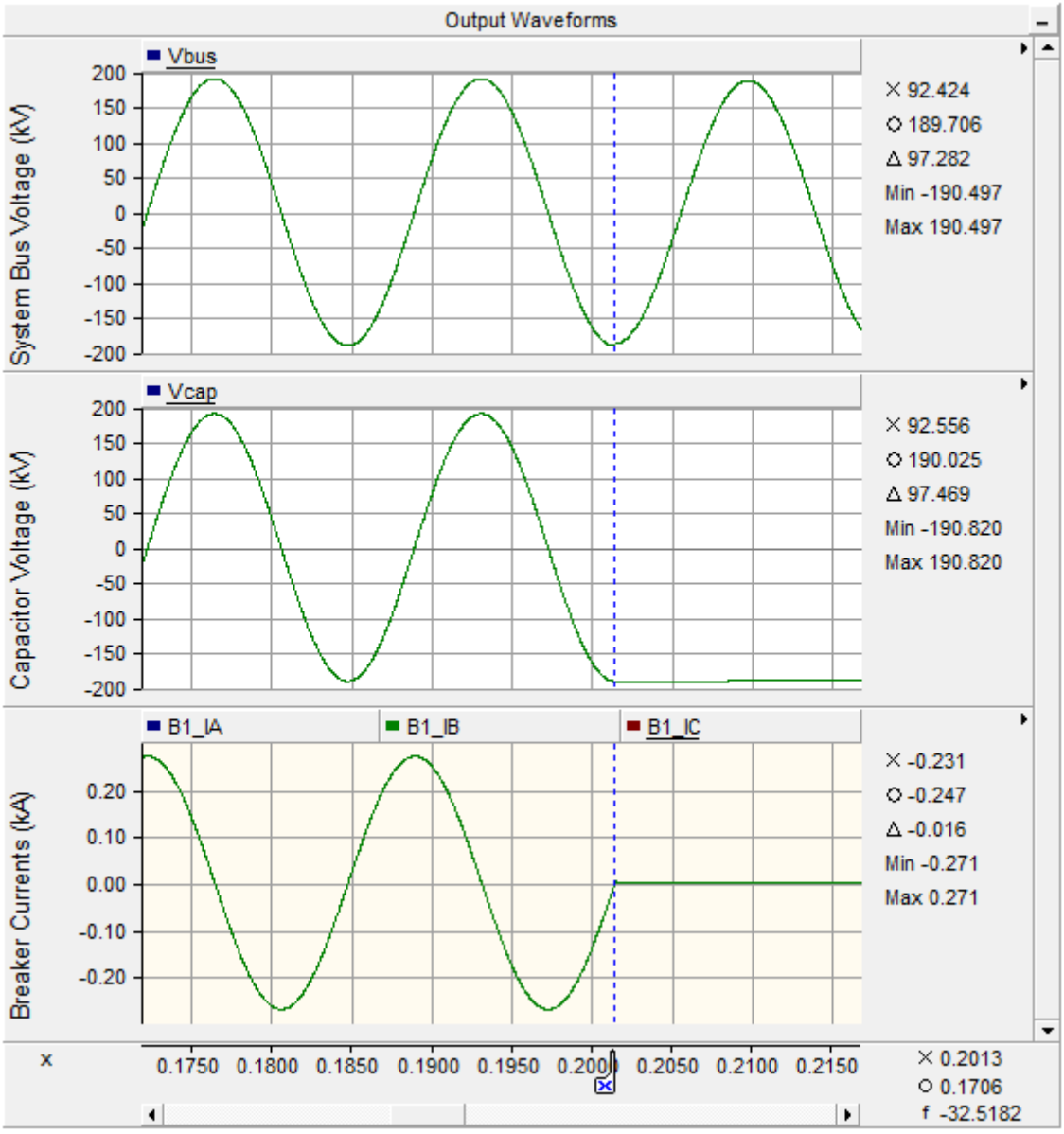


Figure 24: Voltage-Current Relationship of a Capacitor (Phase B)

Note that a half cycle hence from the current interruption, the voltage across the breaker poles is close to twice the system peak voltage, increasing the possibility of a restrike.

The magnitude and frequency of the inrush current and voltage transients can become severe because the capacitor is being re-energized while it still possesses trapped charge. This is unlike previous scenarios, where the capacitor was fully discharged prior to energizing. In the scenarios discussed so far, the voltage across the breaker is approximately $2V_0$ (2 pu). However, if the breaker restrikes a second time during the transient period, the overvoltage can reach up to 3 pu. This

process can repeat itself multiple times, each time increasing the overvoltage. The magnitude and frequency of oscillation of the inrush current due to restrike can be determined as follows:

$$I_{peak} = \frac{\sqrt{(V_0 - V_{cap})^2 - (V_p - V_0)^2}}{Z_{surge}} \qquad 2\text{-}19$$

$$f = \frac{1}{2\pi\sqrt{L_{eq} \cdot C_{eq}}} \qquad 2\text{-}20$$

For the example shown in Figure 23, the following values were determined:

$$L_{eq} = L_{source} + L_{outrush} + L_1 = 0.0265 + 0.00317 + 0.000277 = 0.029947H$$

$$C_{eq} = C_1 = 3.76\mu F$$

$$Z_{surge} = \sqrt{\frac{L_{eq}}{C_{eq}}} = \sqrt{\frac{0.029947}{3.76\mu}} = 89.24\Omega$$

$$V_0 = \sqrt{\frac{2}{3}} \cdot 230k = 187.794kV$$

$V_p = 2 \cdot 180k = 360k$ - Arrestor protective level

Therefore for the worst case situation (V_{cap}= -V_0):

$$I_{peak} = \frac{\sqrt{(187.794k + 187.794k)^2 - (360k - 187.794k)^2}}{89.24} = 3.74kA$$

$$f = \frac{1}{2\pi\sqrt{0.029947 \cdot 3.76\mu}} = 474.3kHz$$

The restrike, in addition to high frequency current transients, will also produce a high-frequency overvoltage. The surge arrestor at the capacitor bank location should be designed to limit the restrike induced overvoltage. Also, the arrestor should be able to absorb the energy associated with the transient without damaging itself.

Objective

The main objective of a re restrike study is to demonstrate that the energy dissipated by the surge arrestor during the event is within its energy rating.

Simulation Results

In this example, the PSCAD multiple-run component is used to re-energize the capacitor at different points along the voltage waveform.

The multiple-run is set up to repeat the simulation approximately 20 times. On each run, breaker B1phase B operates at a different point on the voltage waveform.

All simulation results represent the worst case situation.

Scenario 1

Only a single capacitor was energized prior to restrike. Breaker B1 is initially closed, and breakers B2, B3 and B4 remain open.

The simulation results in Figure 25 show that the inrush current attains a peak value of approximately 4.26 kA and a maximum frequency of about 500 Hz. The simulation follows the hand calculations provided in the Analysis section closely, and these values are within the limits set by the breaker standards.

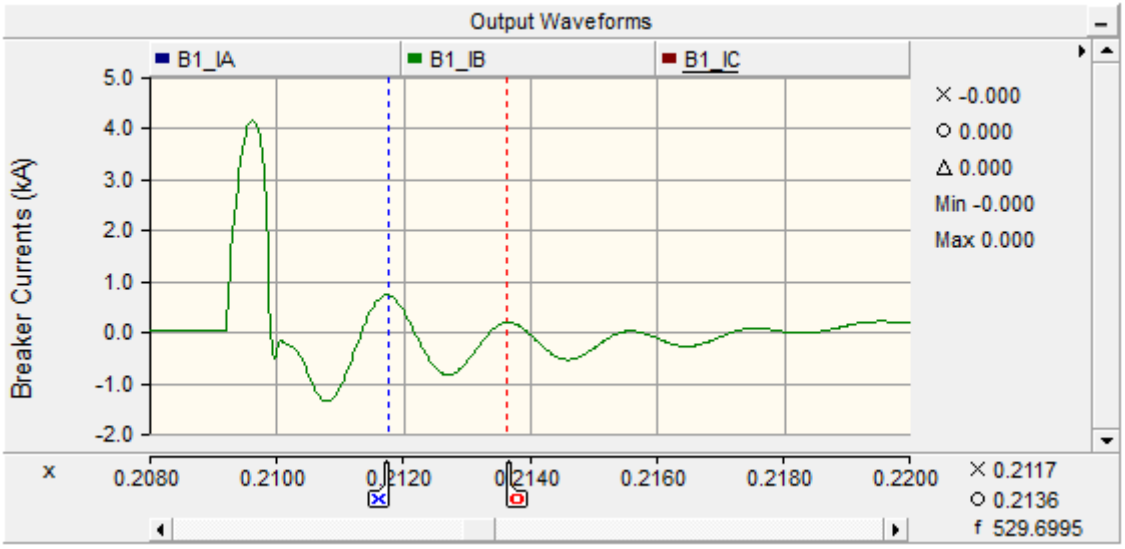


Figure 25: Phase B of the Inrush Current due to Restrike

The simulation results in Figure 26 show that the transient voltage across the capacitor (V_{cap}) attains a maximum peak value of approximately 350 kV (1.87 pu). Prior to restrike, the voltage across the capacitor is held at approximately -188 kV (1 pu). The results also show that the surge arrestor

energy dissipation is around 300 kJ. These values should be compared with the relevant equipment ratings.

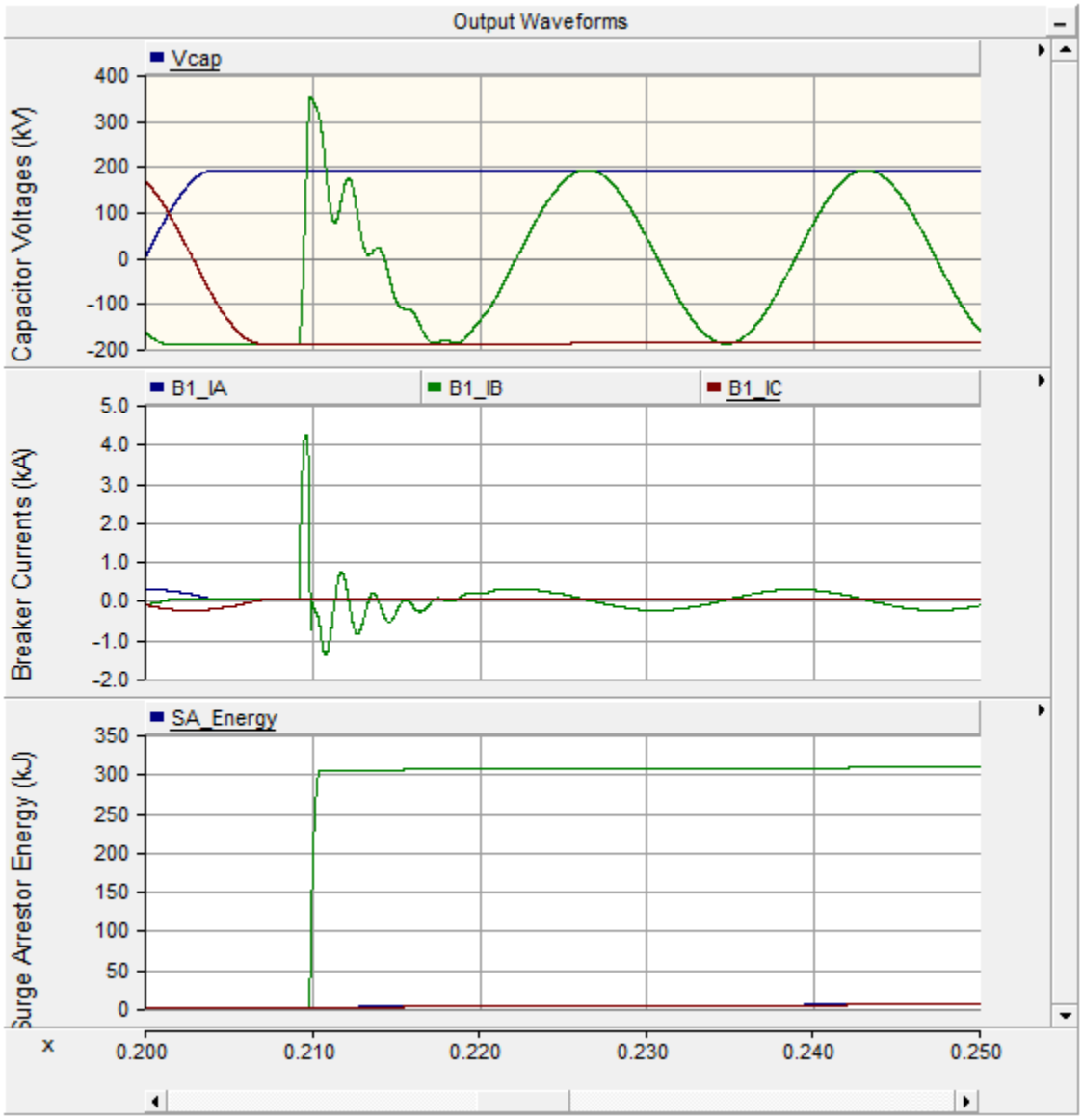


Figure 26: Voltage across Capacitor, Inrush Current and Surge Arrestor Energy

Scenario 2

Two capacitors have been energized prior to restrike. Breaker B1 is initially closed; breaker B2 is closed for the entire simulation and breakers B3 and B4 remain open.

For the worst case situation ($V_{cap} = -V_0$), the peak magnitude and oscillation frequency of the inrush current (hand calculated values) are found using equations 2-19 and 2-20, and are:

$$I_{peak} = 19.44\,kA \qquad f = 4931.58\,Hz$$

The simulation results show that the inrush current attains a peak value of approximately 20 kA and a maximum frequency of 4.8 kHz. The simulations follow the hand calculations reasonably close.

The results also show that the transient voltage across the capacitor (V_{cap}) attains a maximum peak value of approximately 333 kV (1.78 pu). It should be noted that the surge arrestor energy dissipation is around 50 kJ. These values must be compared with the relevant equipment ratings.

Scenario 3

Three capacitors have been energized prior to restrike. Breaker B1 is initially closed, breakers B2 and B3 remain closed for the entire simulation and breaker B4 is open.

The peak magnitude and oscillation frequency of the inrush current (hand calculated values) are found using equations 2-19 and 2-20, and are:

$$I_{peak} = 25.98\,kA \qquad f = 4928.33\,Hz$$

The simulation results show that the inrush current attains a peak value of approximately 29 kA and a maximum frequency of 4.8 kHz. The simulations follow the hand calculations.

Scenario 4

All four capacitors have been energized prior to restrike. Breaker B1 is initially closed, and breakers B2, B3 and B4 remain closed for the entire simulation.

The peak magnitude and oscillation frequency of the inrush current (hand calculated values) are found using equations 2-19 and 2-20, and are:

$$I_{peak} = 29.18\,kA \qquad f = 4931.8\,Hz$$

The simulation results show that the inrush current attains a peak value of approximately 32 kA and a maximum frequency of 4.8 kHz. The simulations follow the hand calculations.

Discussion

Capacitor bank restrike can lead to a severe switching overvoltage at the capacitor bank bus. The surge arrestor should be properly designed to limit such transients.

PSCAD

Refer to case: *cap_bank_study_05.pscx*

References

1. “Modeling and Analysis of System Transients Using Digital Programs”, IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-15.

2.6 Transformer Phase-to-Phase Overvoltage Study

Motivation

The purpose of this study is to illustrate the key points to be considered when energizing a capacitor bank leads to a large phase-to-phase overvoltage at the terminations of a remote transformer. The transformer is connected to the capacitor bank bus via a radial transmission line. A surge arrestor is used to limit the overvoltage to ensure it does not exceed the transformer rating.

System Overview

A Thévanin equivalent voltage source representing a 230 kV system is connected to a 60 km, 230 kV transmission line and a 75 MVAr (25 MVAr per phase – 3.76 µF) capacitor bank. The transmission line is terminated by a 100 MVA, 230/69 kV transformer and the LV-side of the transformer is open-circuited.

The phase-to-phase voltages (V_{ab}, V_{bc} and V_{ca}) at the high voltage terminal of the transformer are the focus of this study (see Figure 27).

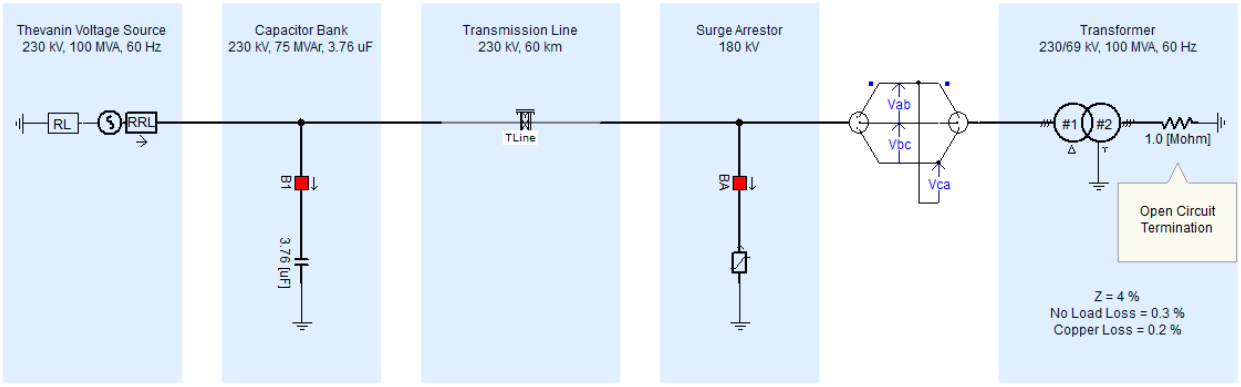


Figure 27: A 230 kV Thévanin Source Connected to a 60 km Transmission Line and Capacitor Bank

The capacitor bank will be energized by closing the circuit breaker B1. This will create a travelling wave, which propagates down the 60 km transmission line. At the transformer HV terminals, the magnitude of the travelling wave will increase due to reflection. This creates a significant overvoltage, which can damage the transformer. The worst case will occur when two phases, phase A and phase B, have a magnitude of 2 pu but opposite polarity. This will result in a phase-to-phase voltage (V_{ab}) of 4 pu [1]. A surge arrestor is placed just before the transformer terminals to ensure the transient voltage does not reach excessive levels, thereby protecting the transformer.

Surge Arrestor

The rated voltage of the surge arrestor (connected from line to ground) in this example is 180 kV, which is typical for a 230 kV system. The surge arrestor characteristics are similar to those found in Section 2.4.

Transmission Line data

Typical data corresponding to a 230 kV line is used in this example simulation (see Figure 28 and Table 2).

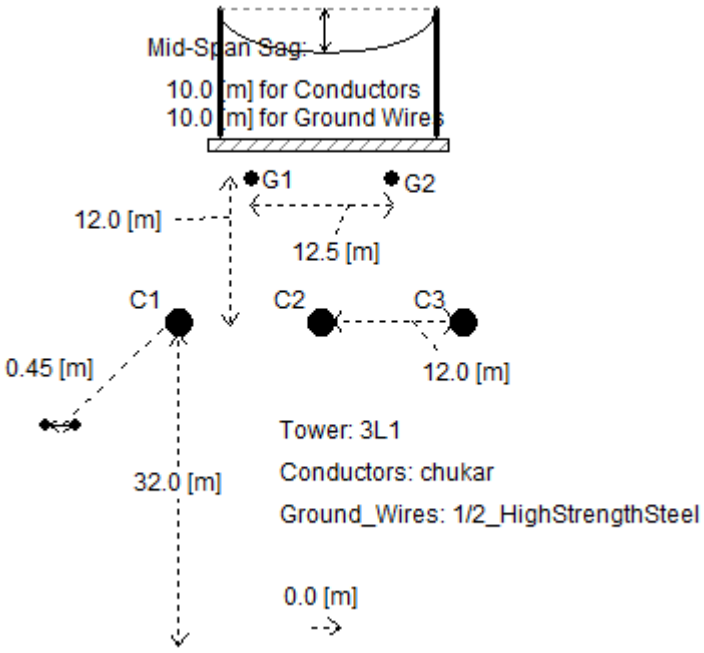


Figure 28: Conductor Heights and Spacing

Conductor outer radius	**0.015 m**
Conductor dc resistance	0.06 Ω/km
Sub-conductors per bundle	2 (symmetrical)
Bundle spacing	0.45 m
Ground wire radius	0.005 m
Ground wire dc resistance	0.06 Ω/km

Table 2: Conductor Data

Line length and conductor characteristics are key contributions to this phenomenon.

> **Note**
> For very short transmission lines, a larger overvoltage may occur as transformer internal resonance may be triggered. This phenomena is not studied in this simulation [1].

Objectives

The main objectives of a transformer phase-to-phase overvoltage study are to demonstrate that:

- The transient overvoltage is well damped and that the magnitudes do not violate the temporary overvoltage capability of the transformer.

- The peak magnified transient voltage is less than the rating of the transformer insulation levels.

Simulation Results

In this example, the PSCAD multiple-run component is used to energize the capacitor at different points along the voltage waveform. The multiple-run unit is set up to repeat the simulation approximately 20 times. On each run, breaker B1 closes at a different point on the voltage waveform.

Scenario 1

The surge arrestor is not present.

The simulation results in Figure 29 represent the worst case situation when the surge arrestor is not used to limit the voltage. The transient phase-to-phase voltage reaches a peak value of approximately 850 V (2.6 pu).

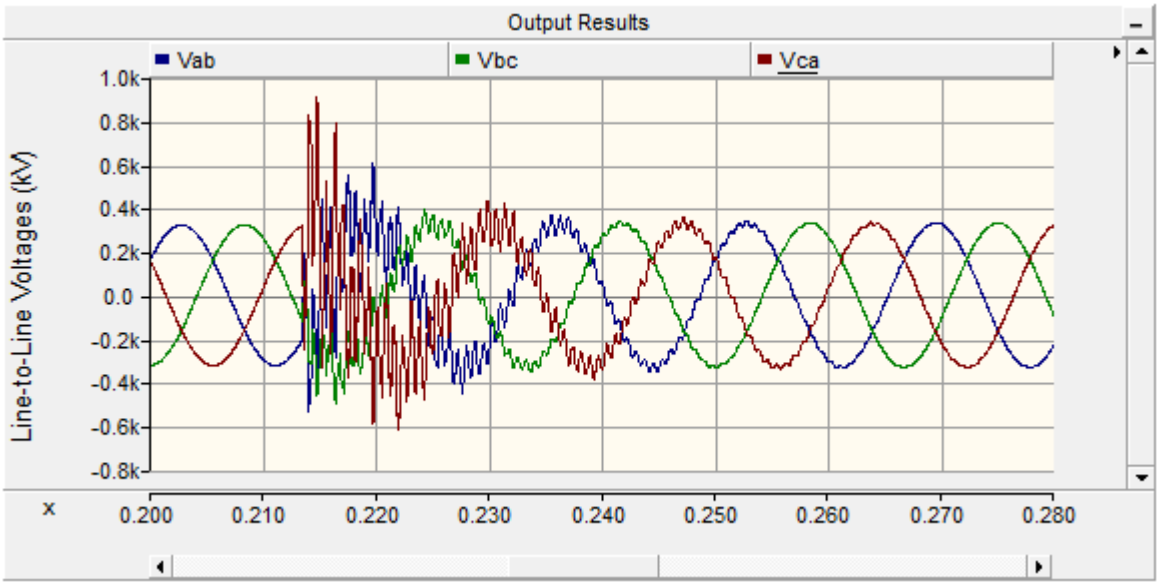


Figure 29: Phase-to-Phase Overvoltage without the Surge Arrestor

For the sake of comparison, the switching of a 75 MVAr (1.87 H) reactor at the 230 kV bus was simulated. Figure 30 shows the results. No transients are observed at the transformer terminal 60 km away.

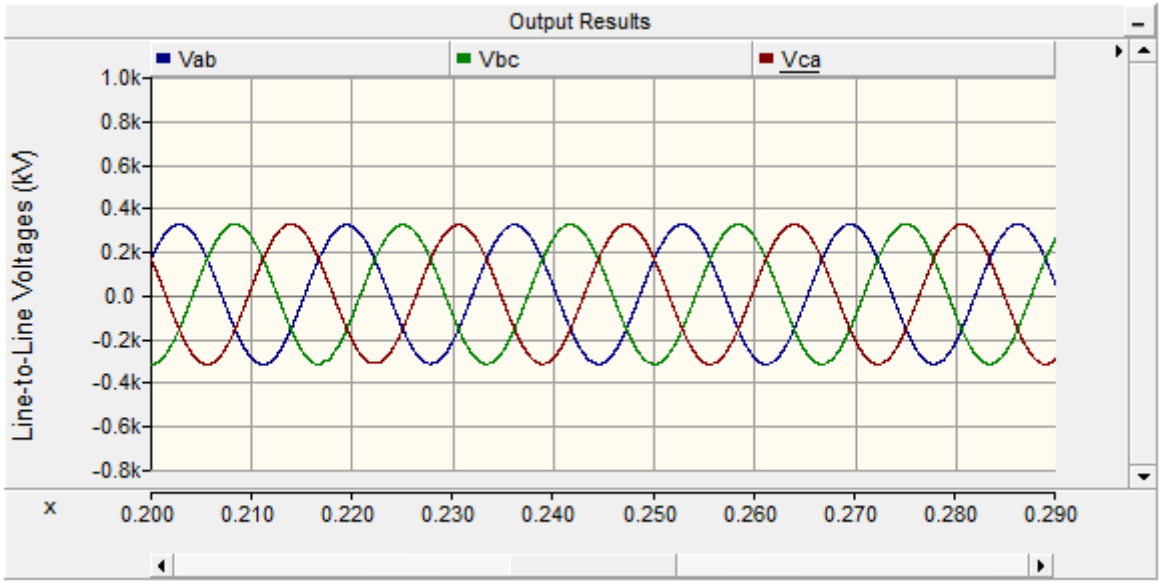


Figure 30: Phase-to-Phase Overvoltage with a 75 MVAR Reactor

Scenario 2

The surge arrestor is present.

The simulation results in Figure 31 represent the worst case situation when the surge arrestor is used to limit the voltage. The transient phase-to-phase overvoltage reaches a peak value of approximately 600 V (1.9 pu).

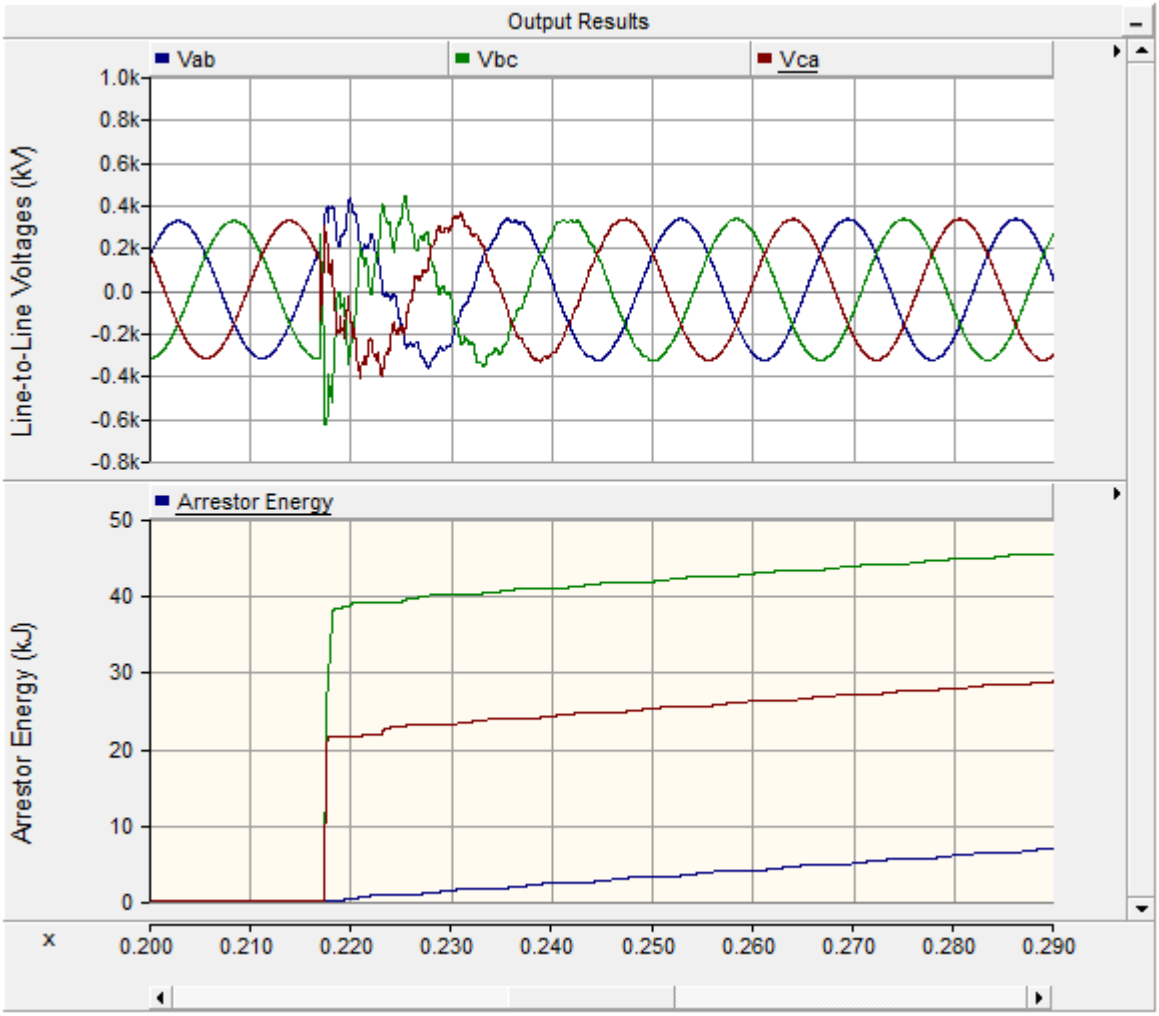


Figure 31: Simulation Results with the Surge Arrestor Present

Discussion

Depending on the length of the transmission line, the worst case overvoltage can reach a magnitude of up to 4 pu.

Adding a surge arrestor is the most effective method to mitigate the transients. However, mitigation methods such as synchronous closing or pre-insertion resistors/inductors are also applicable.

PSCAD

Refer to case: *cap_bank_study_06.pscx*

References

1. “Modeling and Analysis of System Transients Using Digital Programs”, IEEE Publication No. TP-133-0, Piscataway, NJ: IEEE, 1998, pp. 4-14 to 4-15.

DOCUMENT TRACKING

Rev.	Description	Date
0	Initial	01/Jun/2013
1	Update to New Brand Guidelines	08/May/2018

Copyright © 2018 Manitoba Hydro Internal Ltd. All Rights Reserved.