MANITOBA·HVDC RESEARCH CENTRE

Webinar:

MMC- Technologies

Presenters: Juan Carlos Garcia and Farid Mosallat

February 26 - 2015

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If you have questions during the Webinar

- Please e-mail PSCAD Support at

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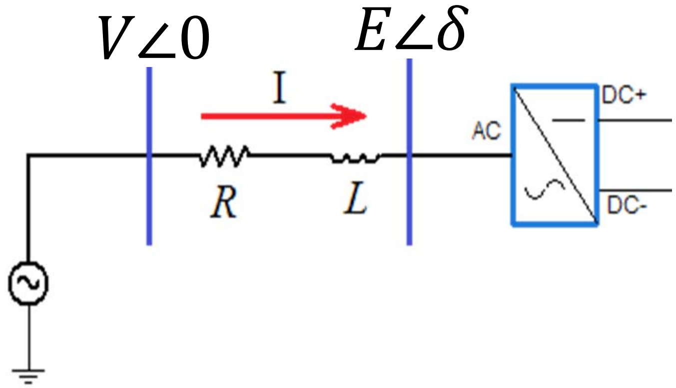
Grid-connected VSC: Operation principle



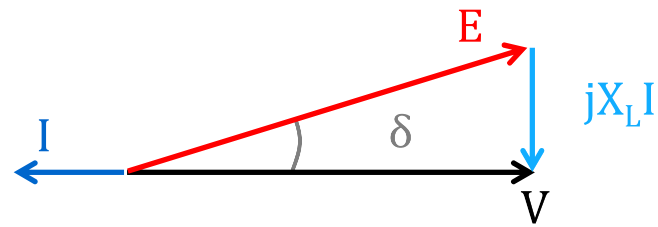
Neglecting R:

$$I = \frac{V\angle 0 - E\angle\delta}{jX_L}$$

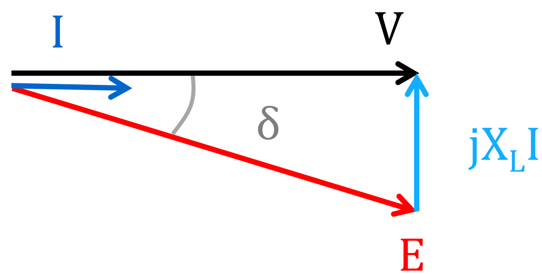
$$S = VI^* \Rightarrow$$

$$\begin{cases} P = -\dfrac{EV}{X_L}\sin(\delta) \\ Q = \dfrac{V^2 - EV\cos(\delta)}{X_L} \end{cases}$$

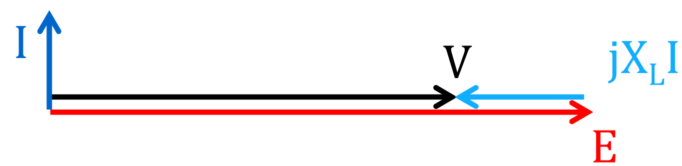
Supplying P:



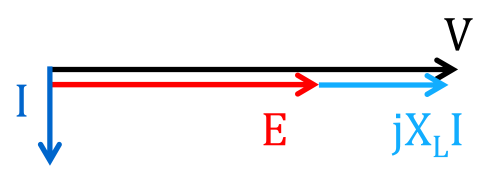
Absorbing P:



Supplying Q:

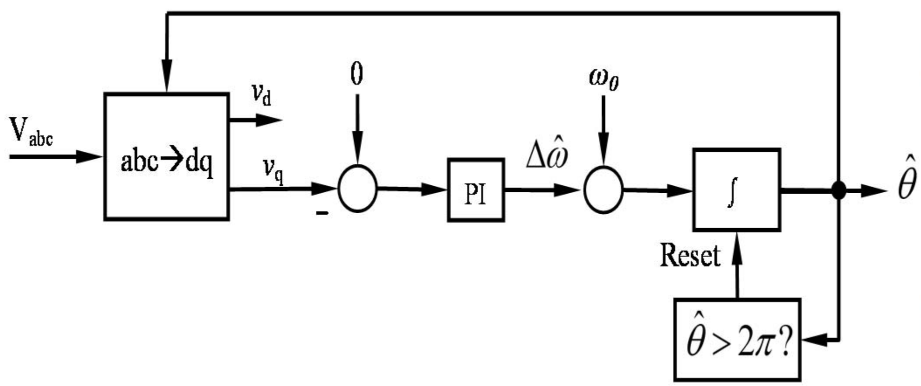


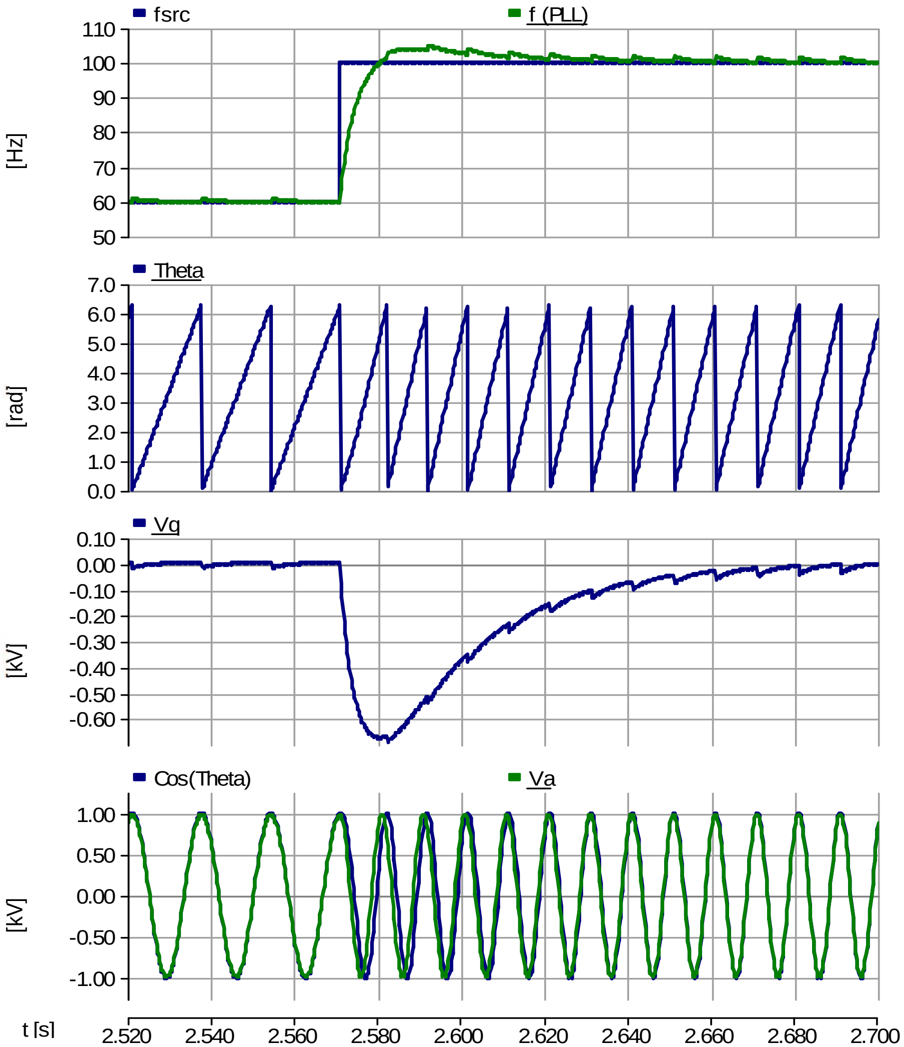
Absorbing Q:



Phase Locked Loop (PLL)

Extracting the phase angle of phase-A voltage





Control modes for grid-connected operation

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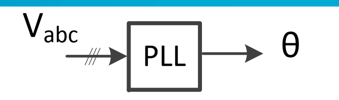
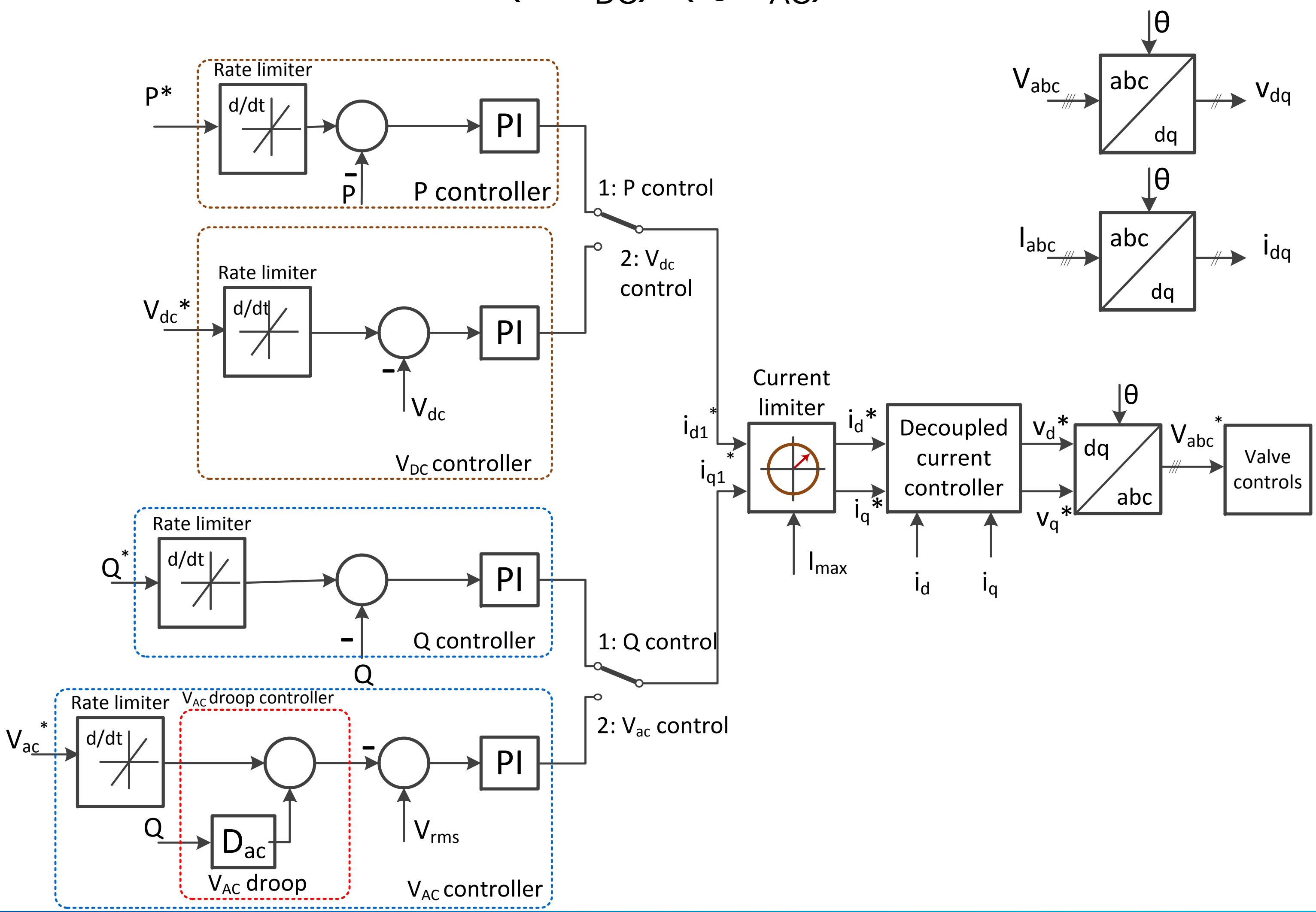
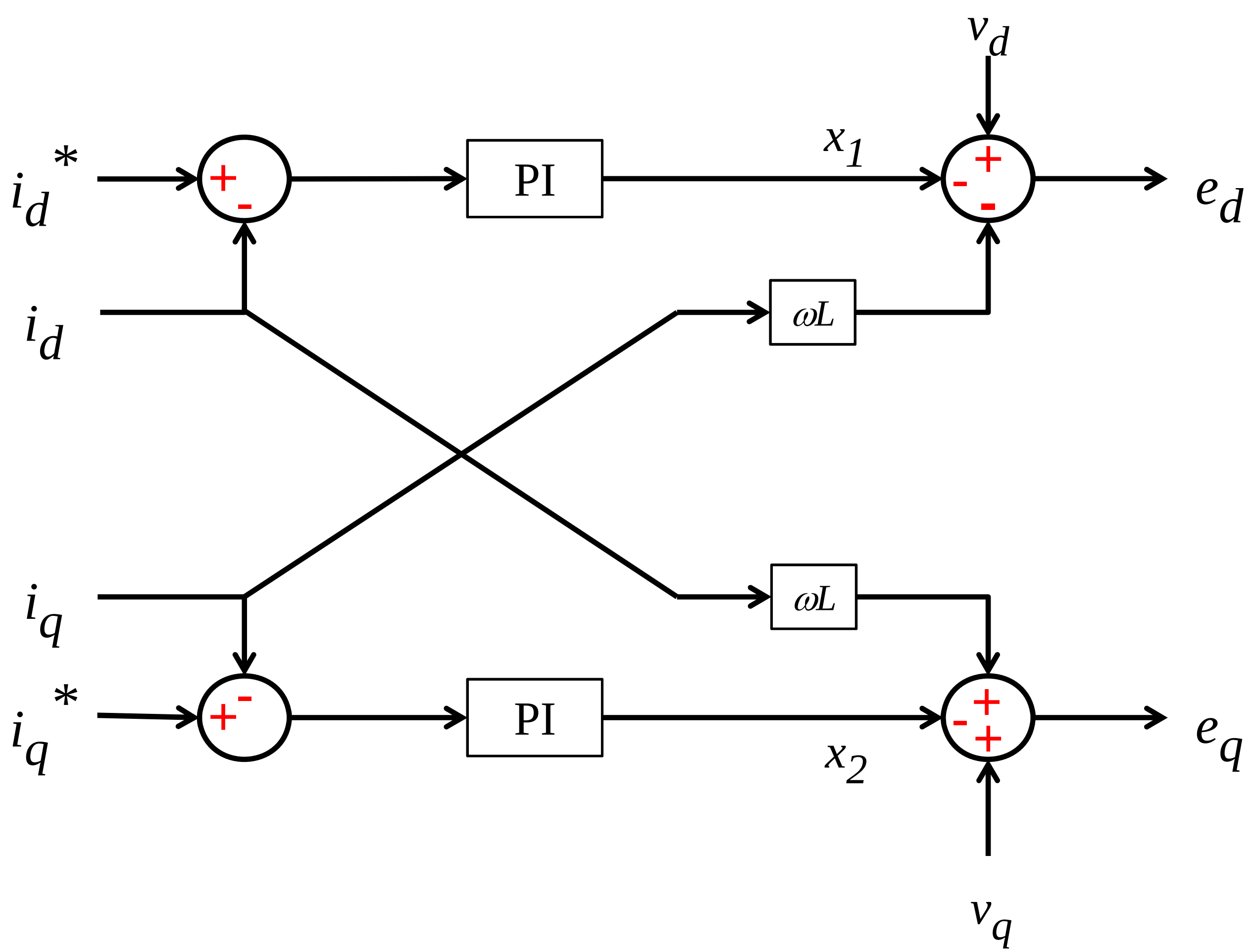
Basic control modes: (P/V_{DC}), (Q/V_{AC})



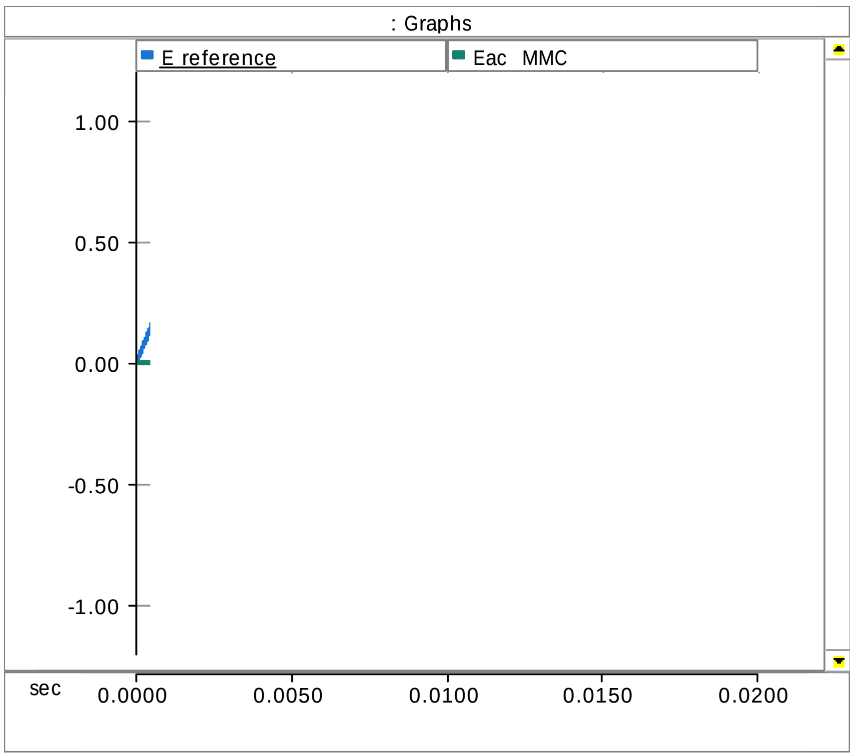


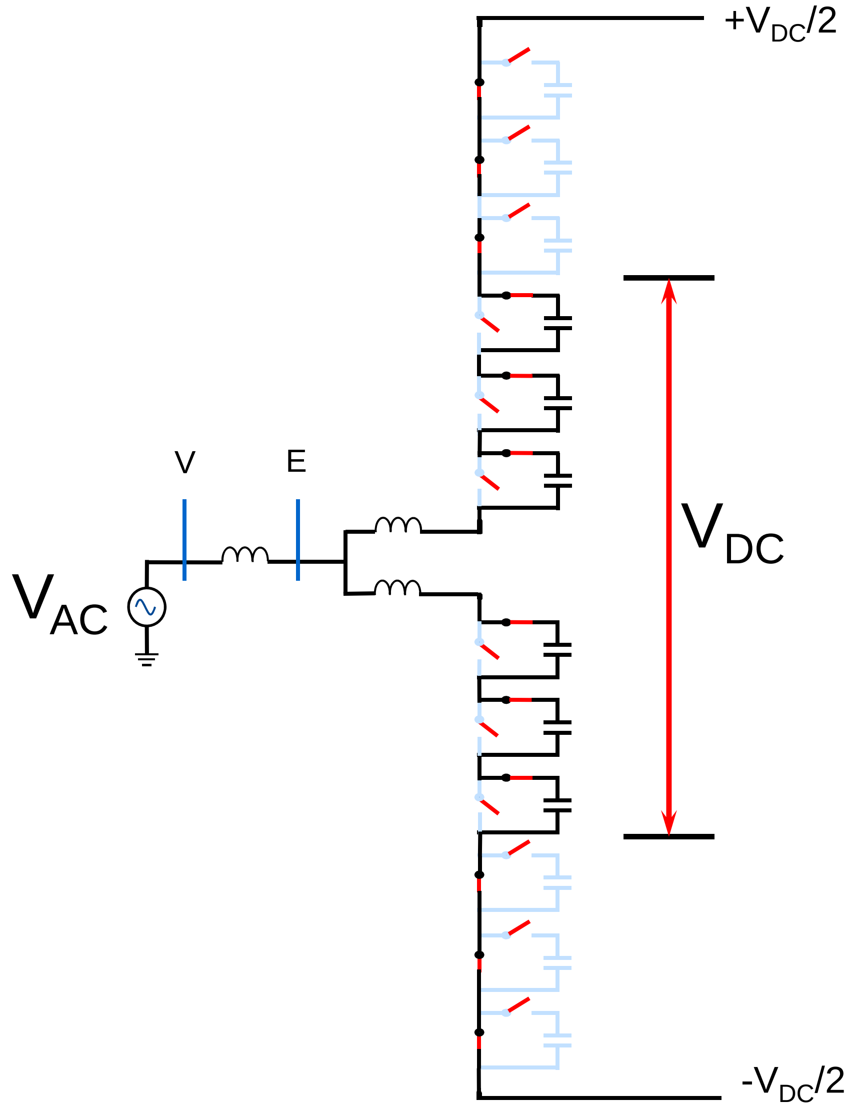
Decoupled current control strategy

Current vector control with PLL locking to phase A voltage (cosine function)

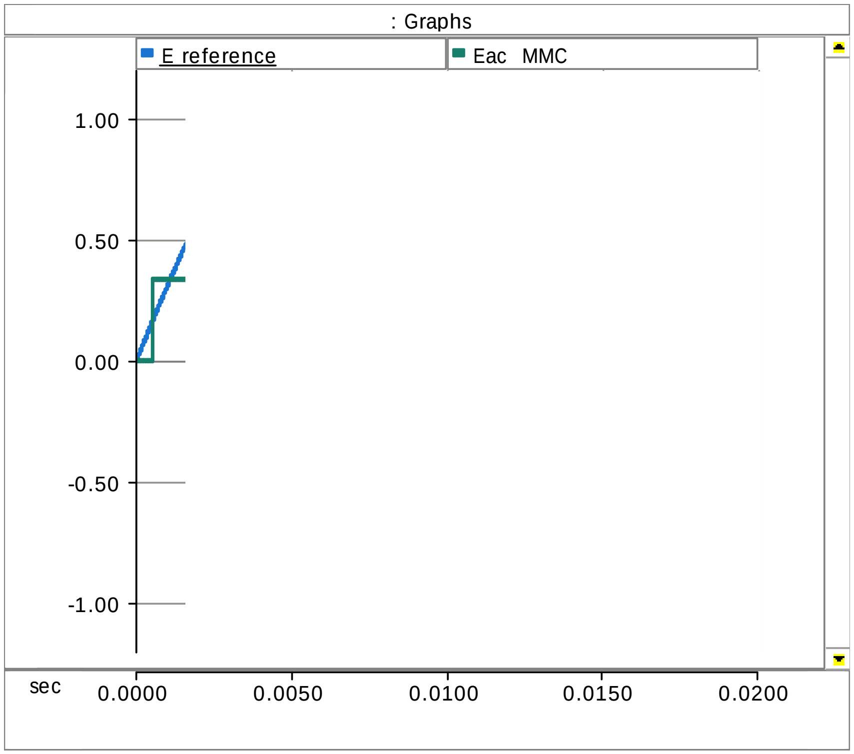


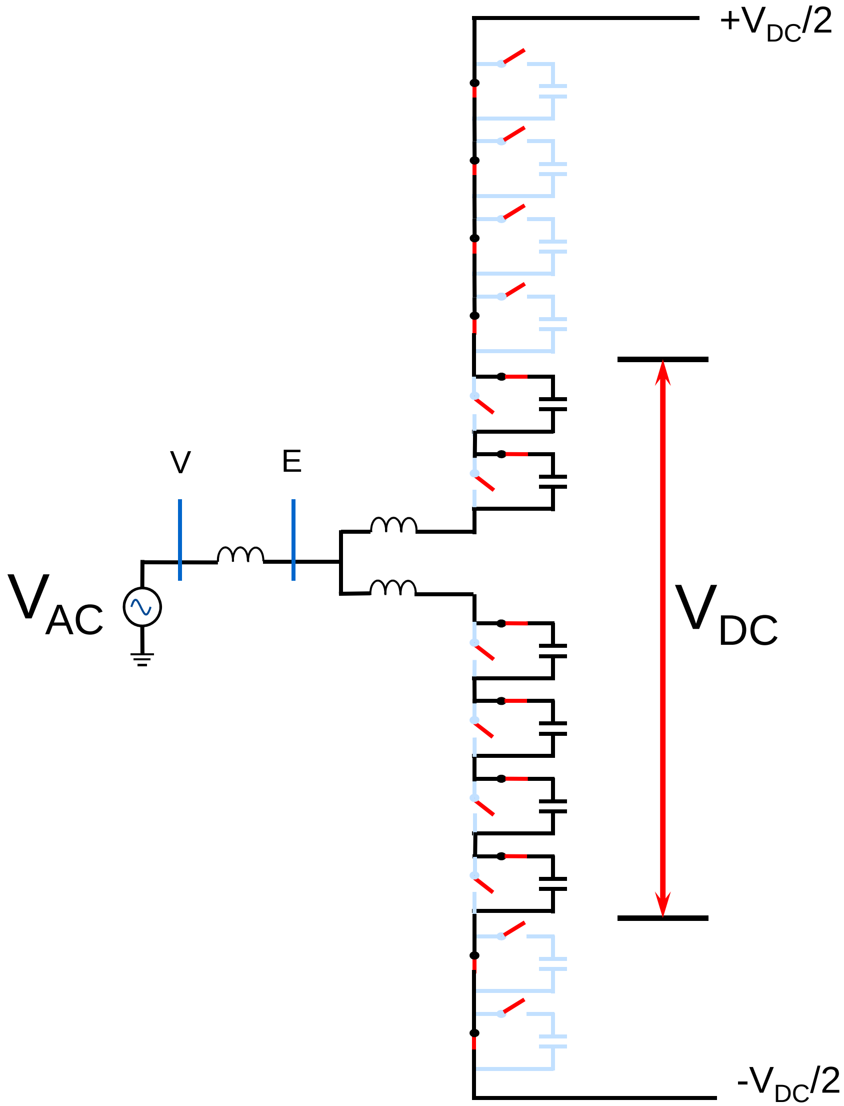
Modular multilevel converters





Modular multilevel converters





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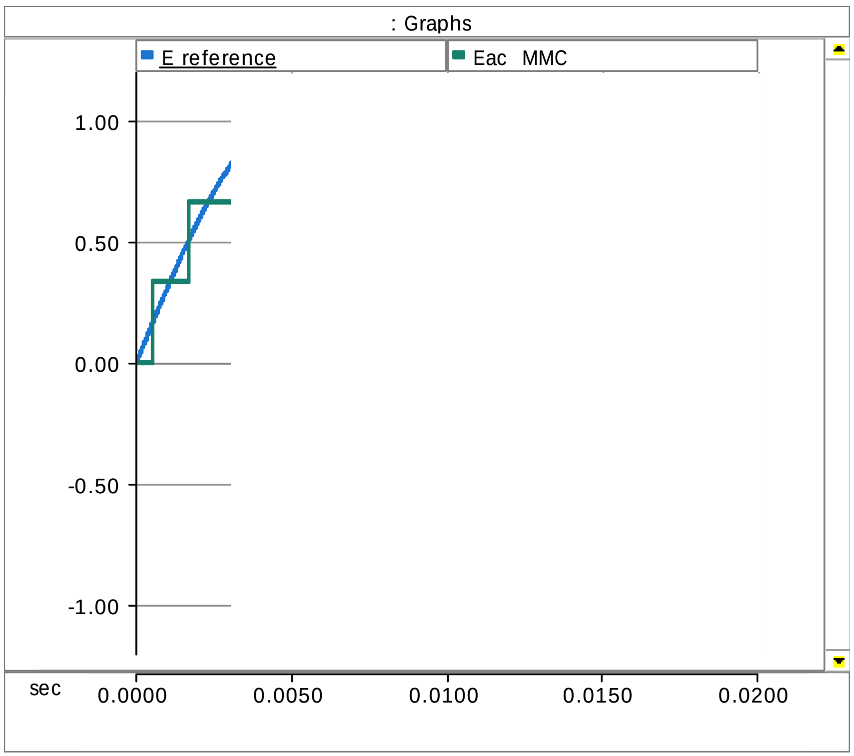
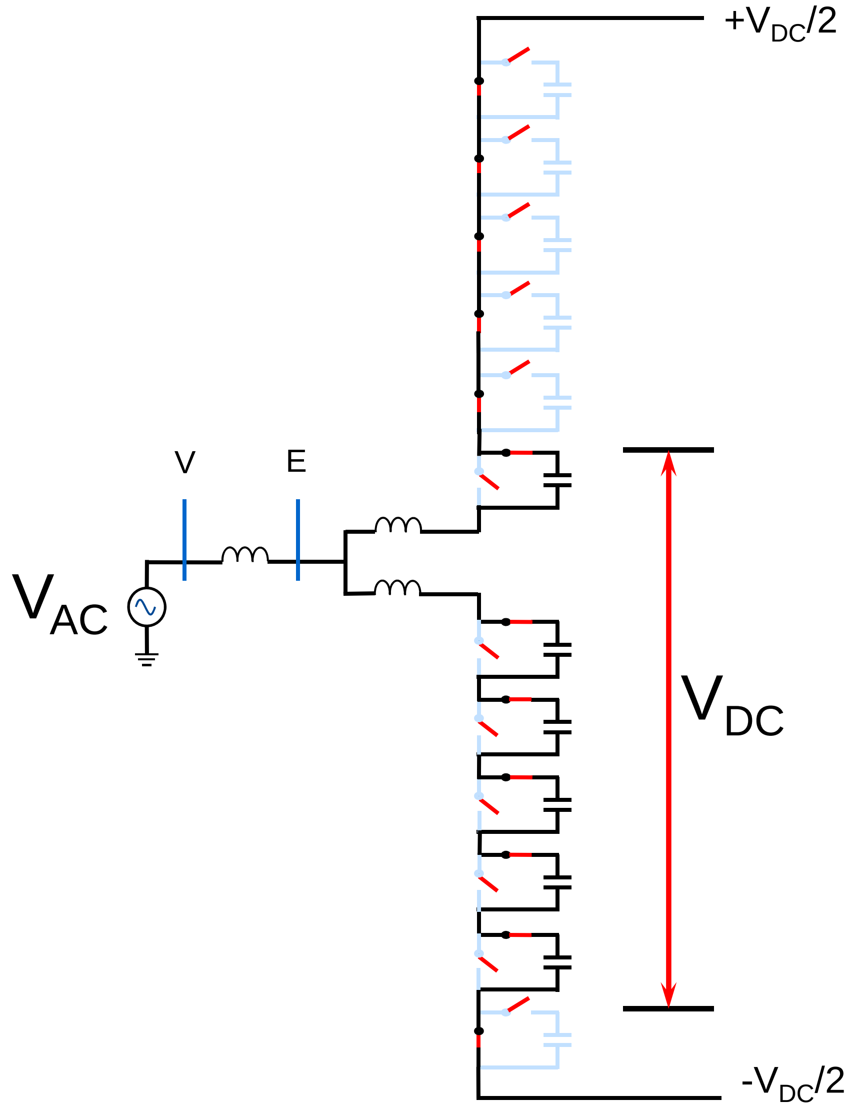
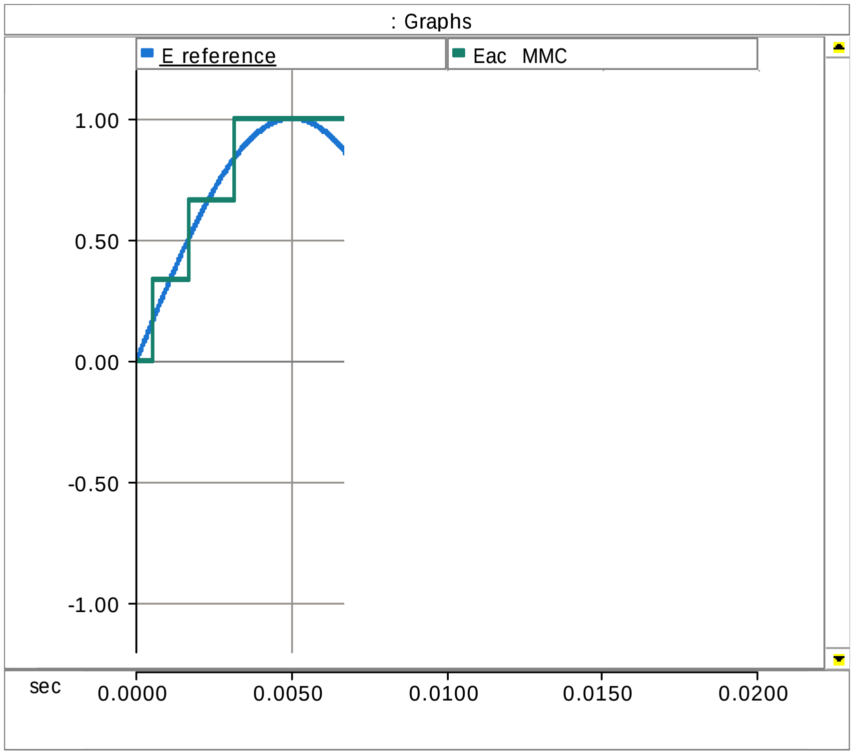
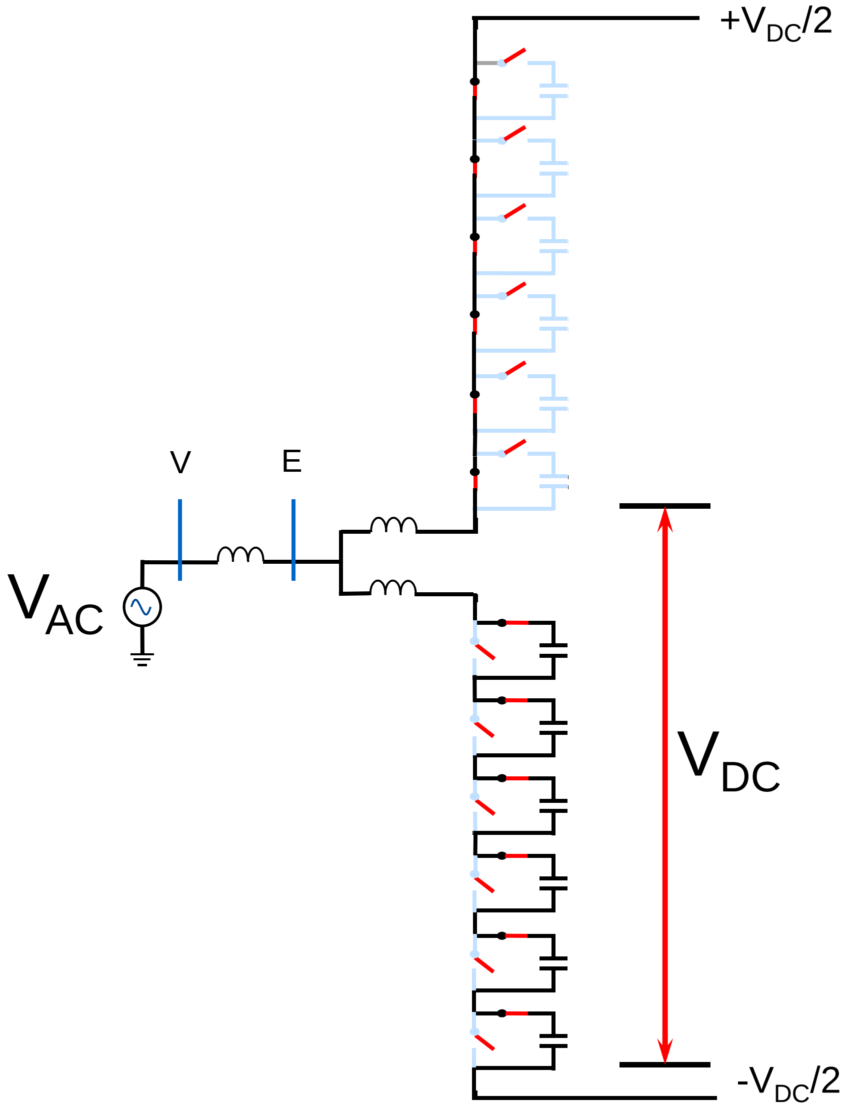




Modular multilevel converters





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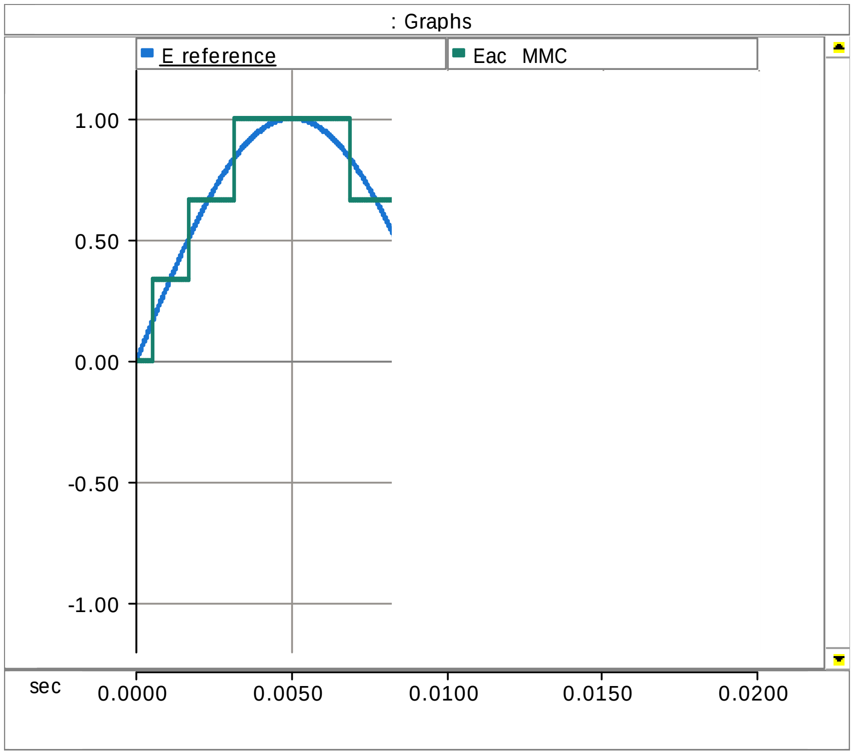

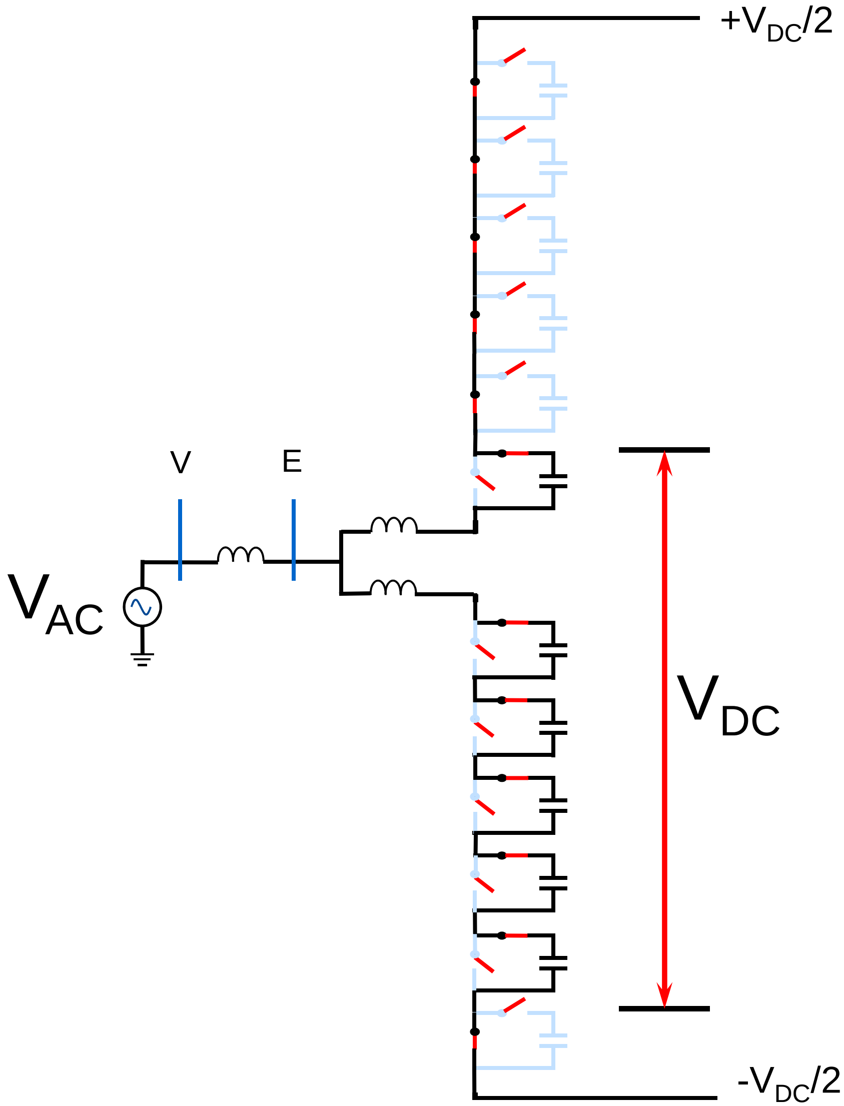

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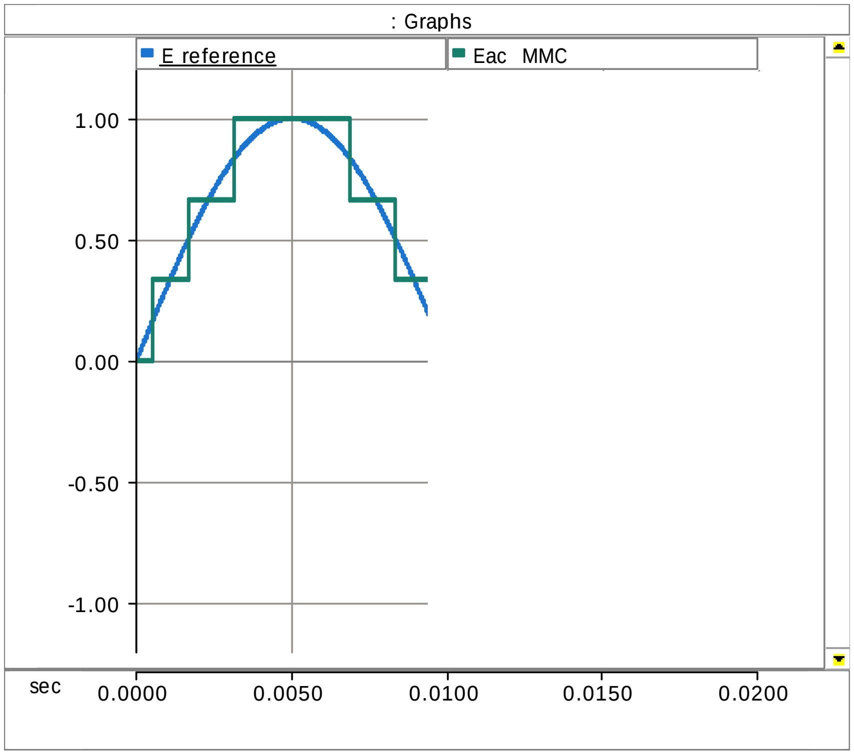

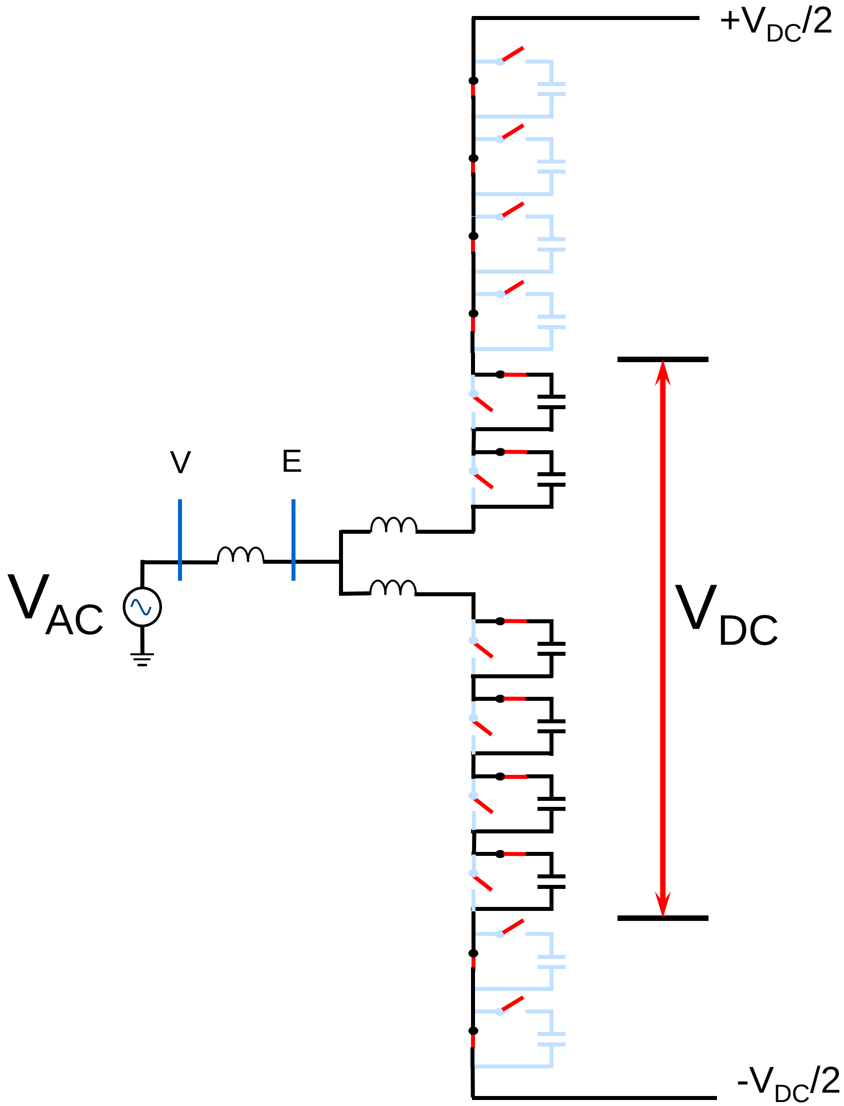

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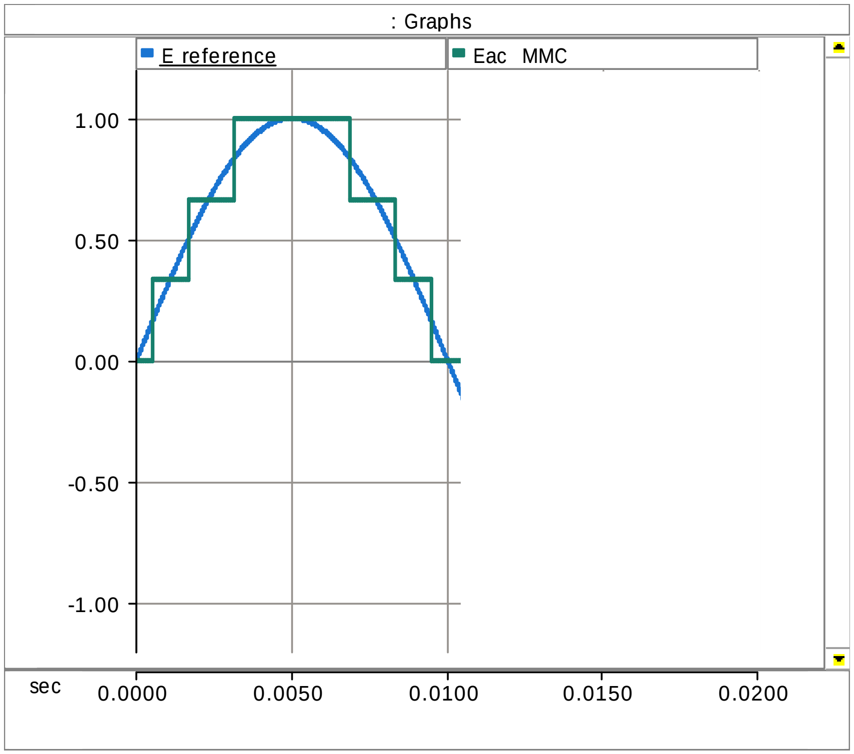

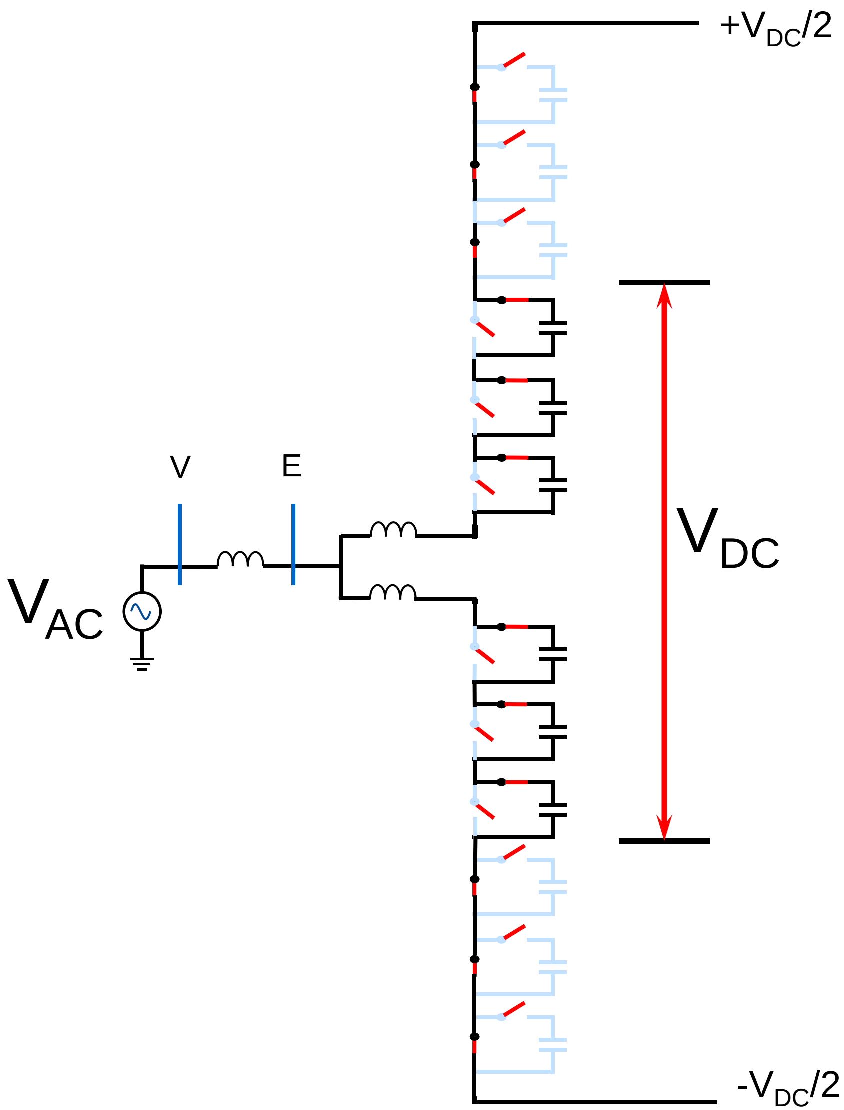

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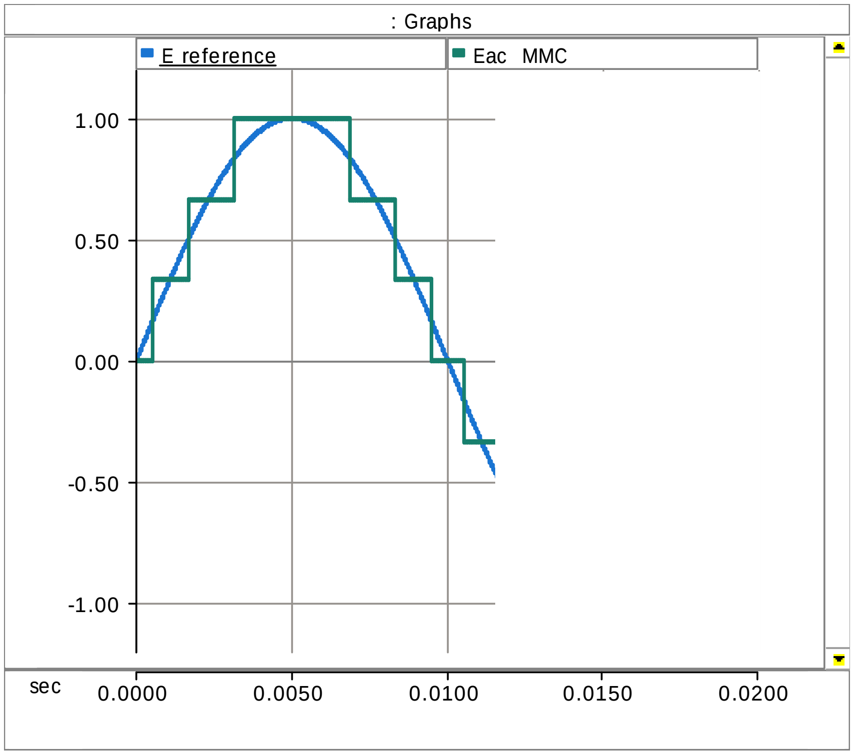

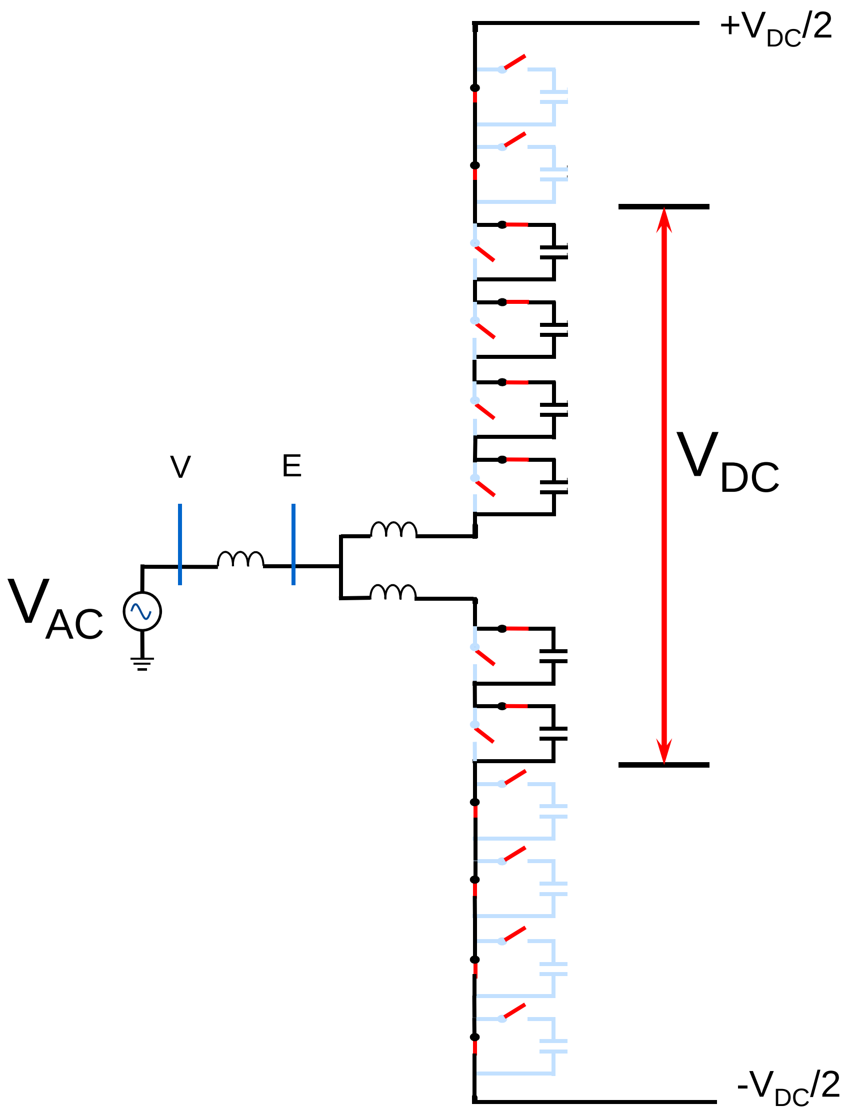

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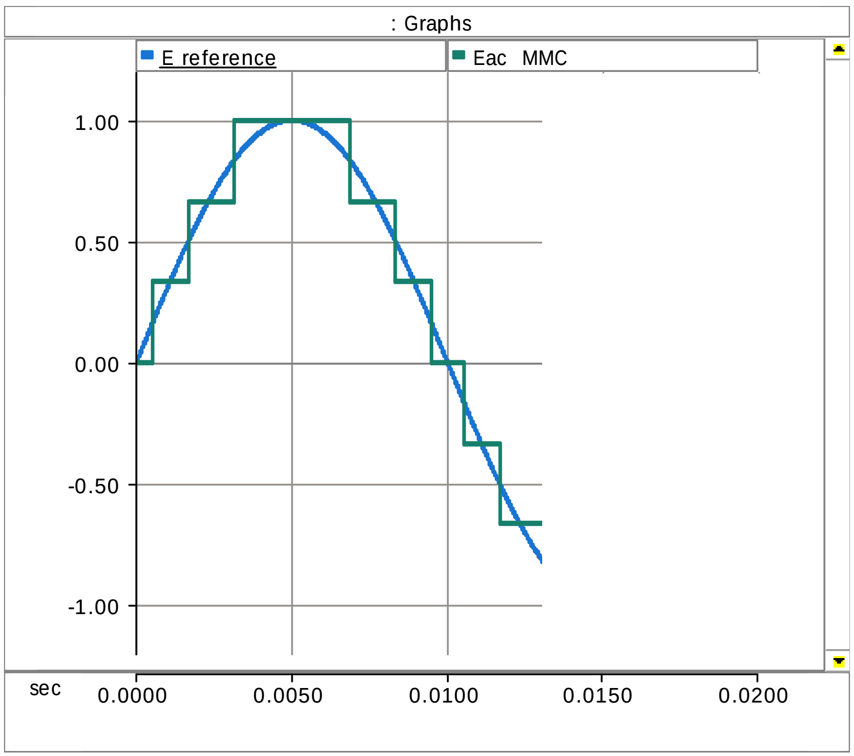

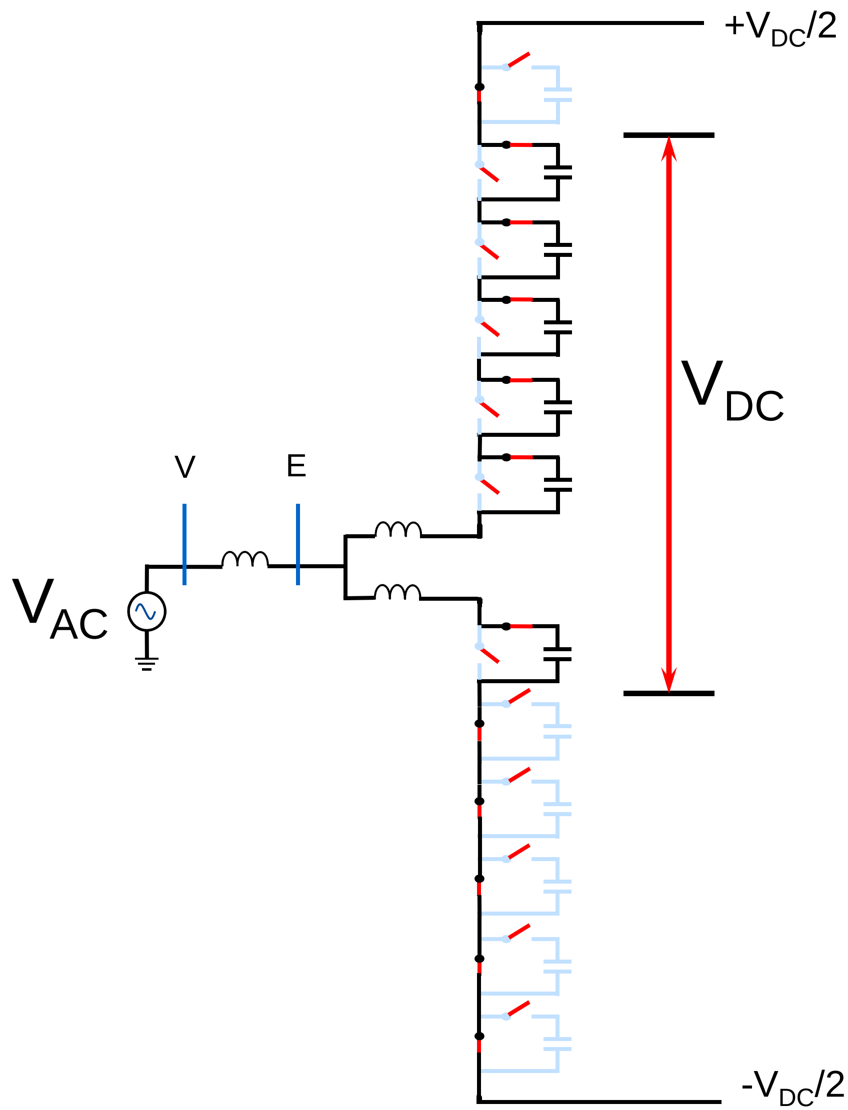

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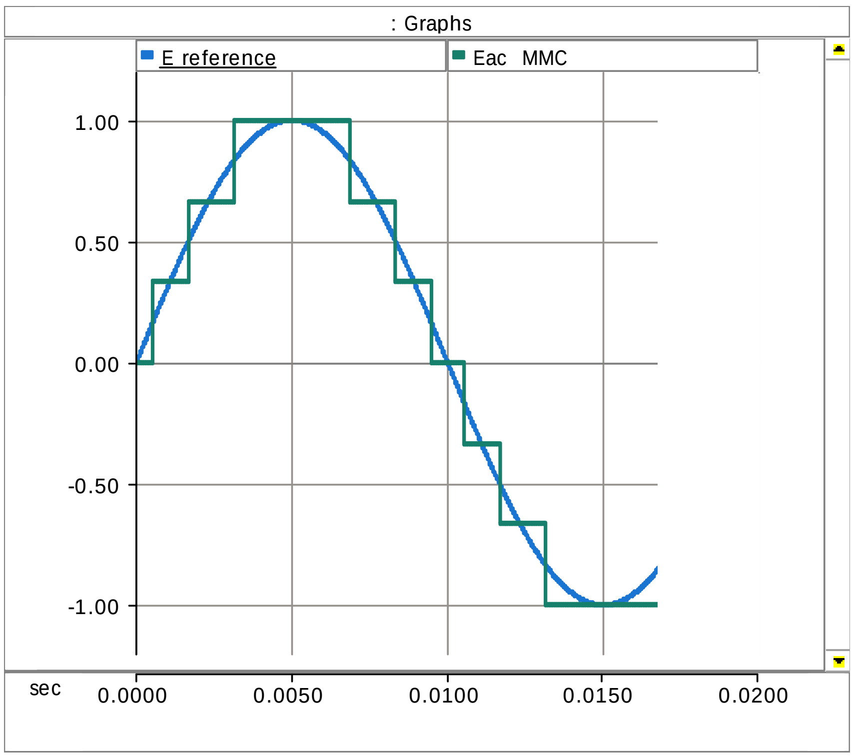

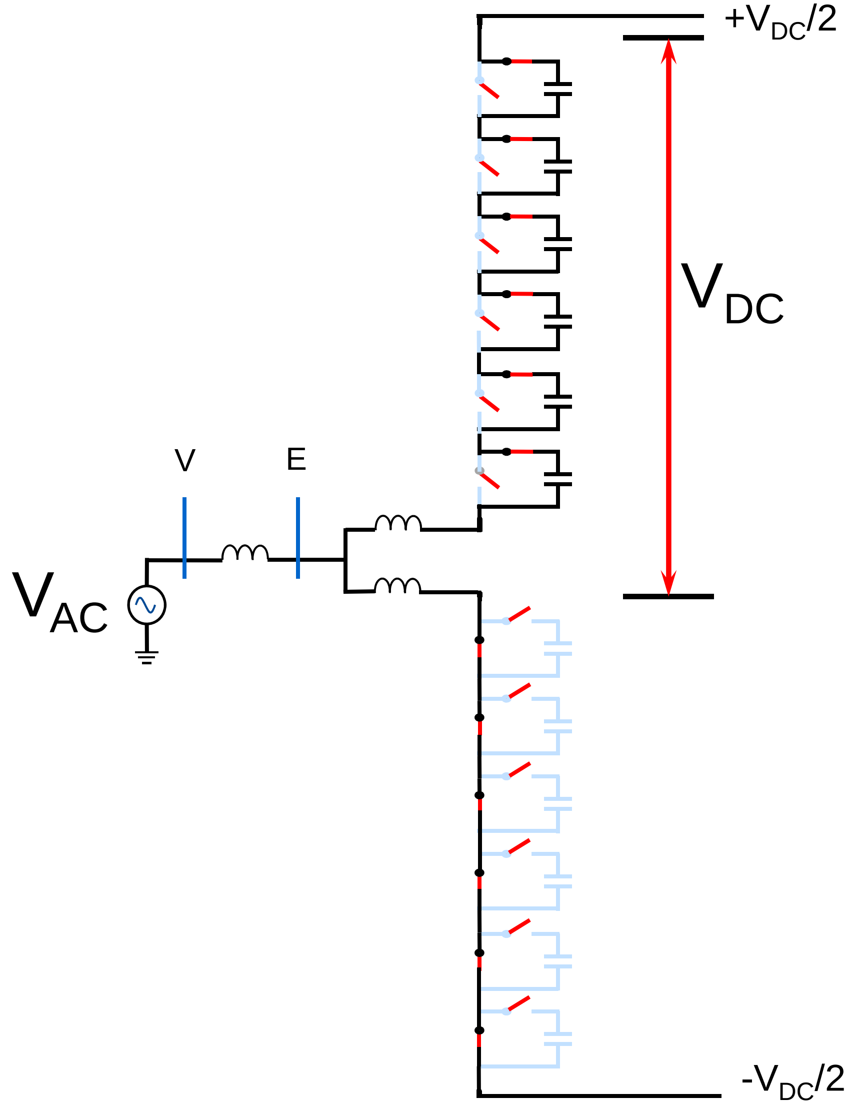

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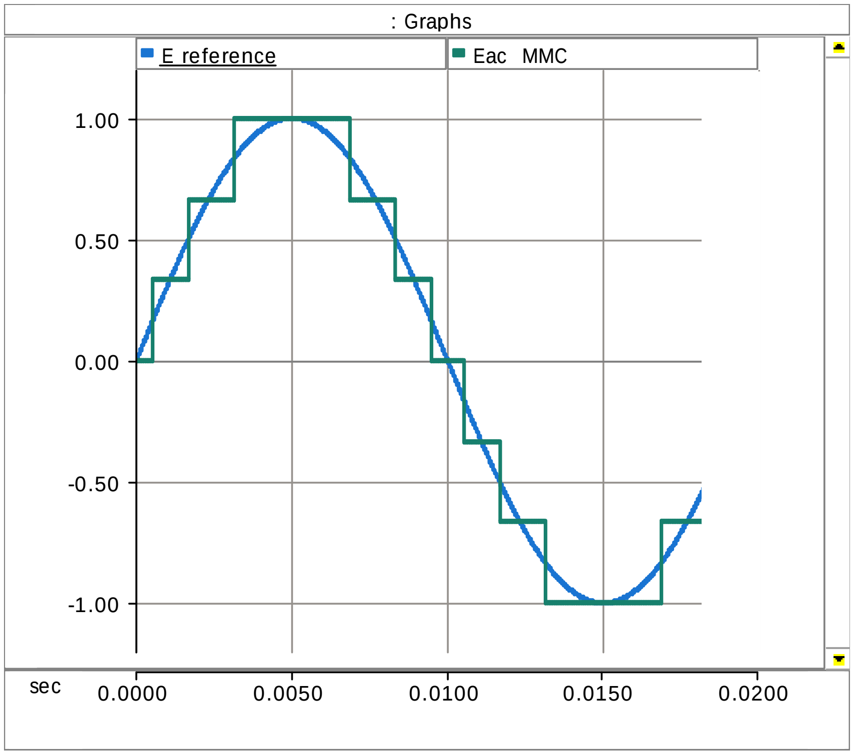
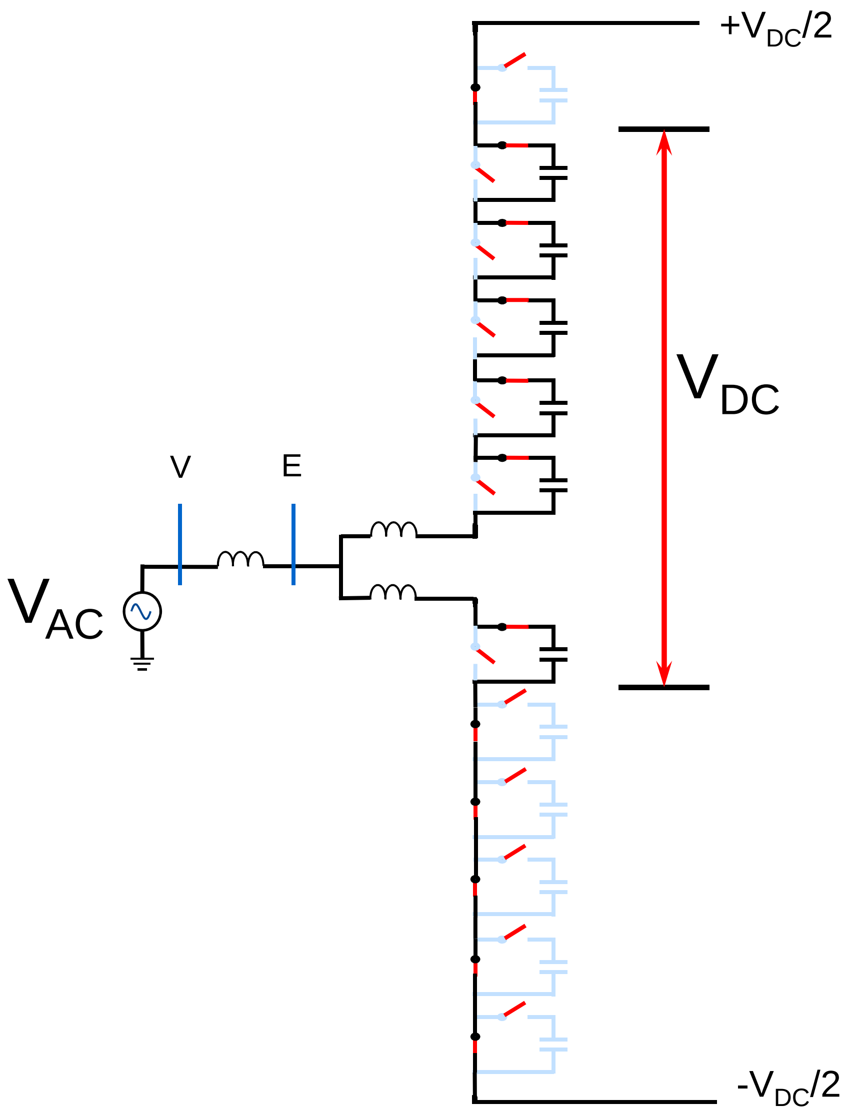
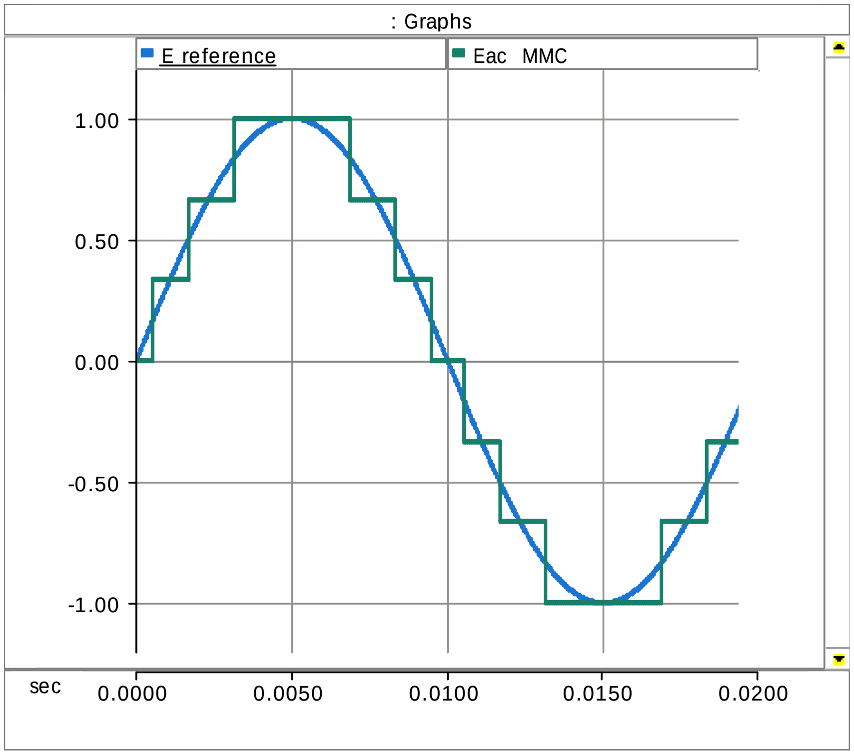
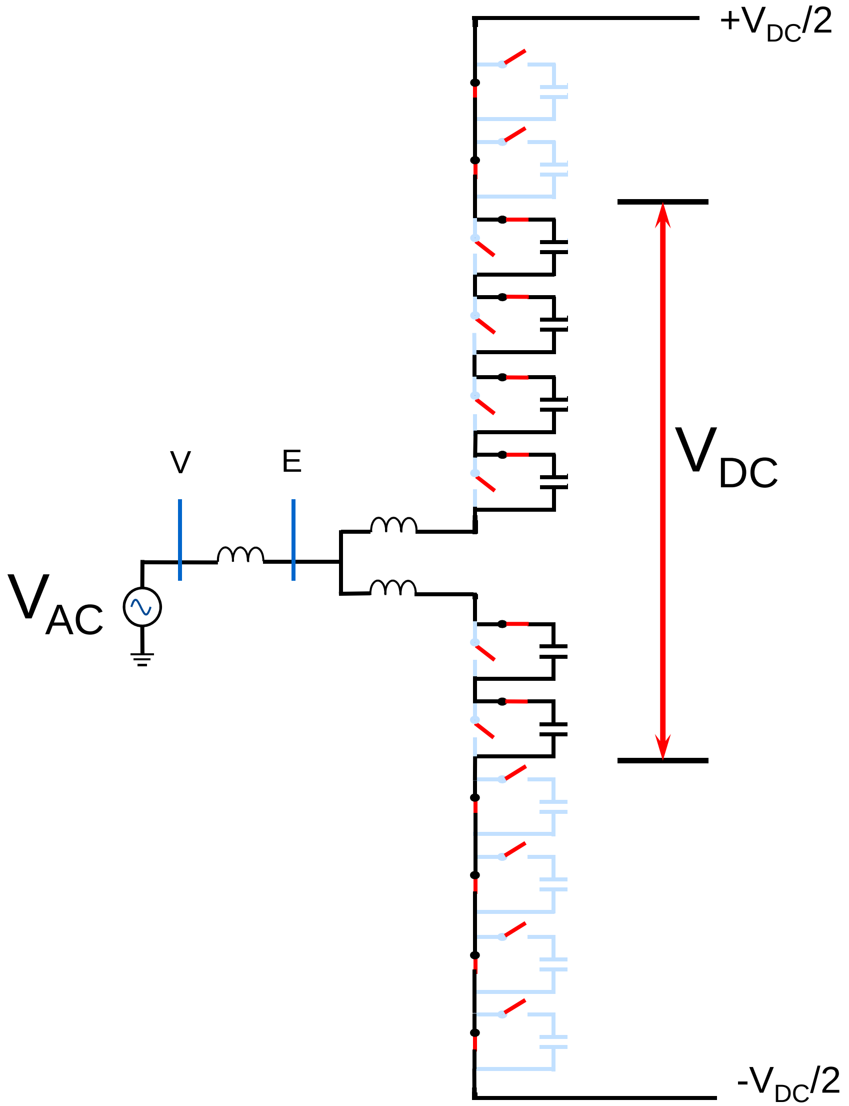


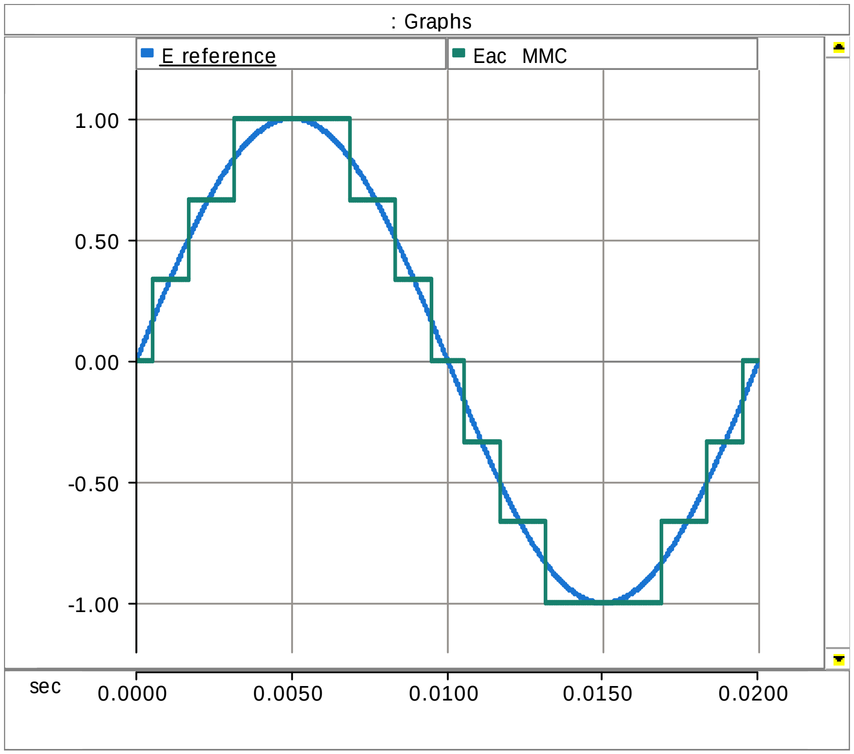


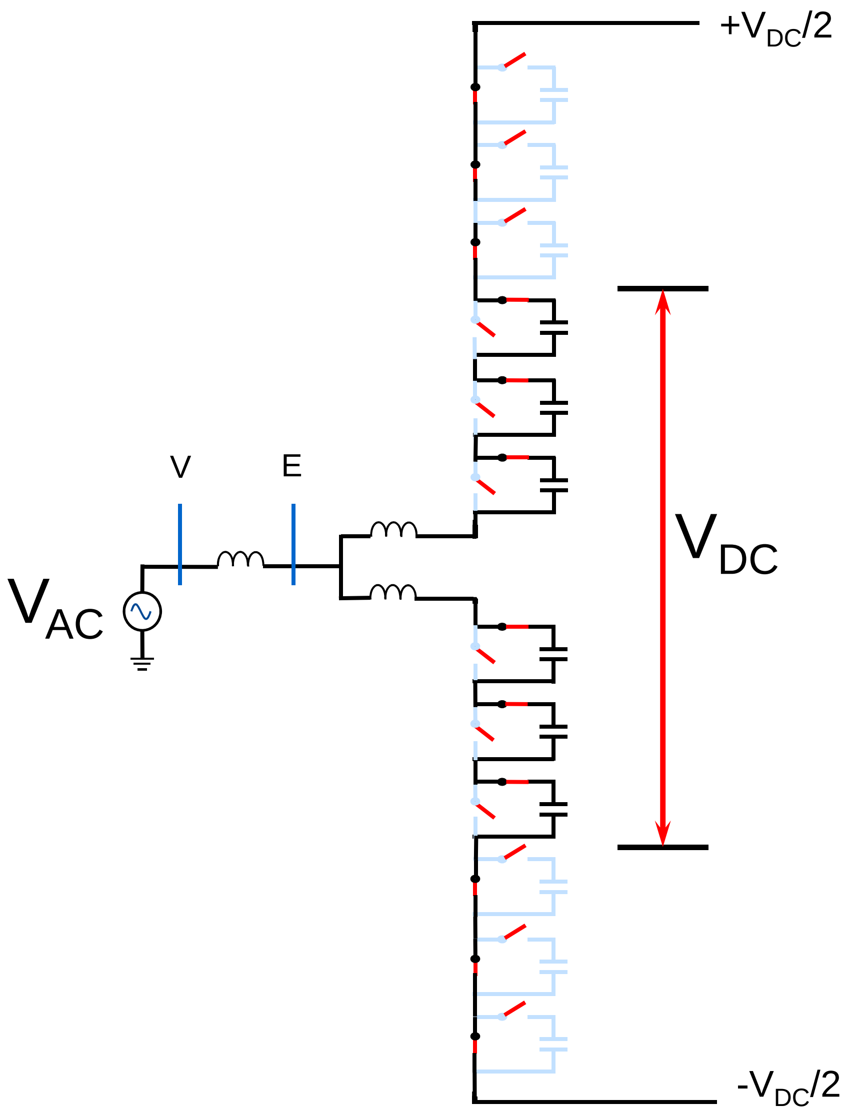
Modular multilevel converters





Modular multilevel converters

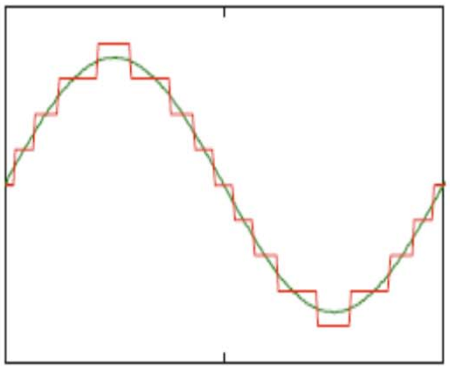


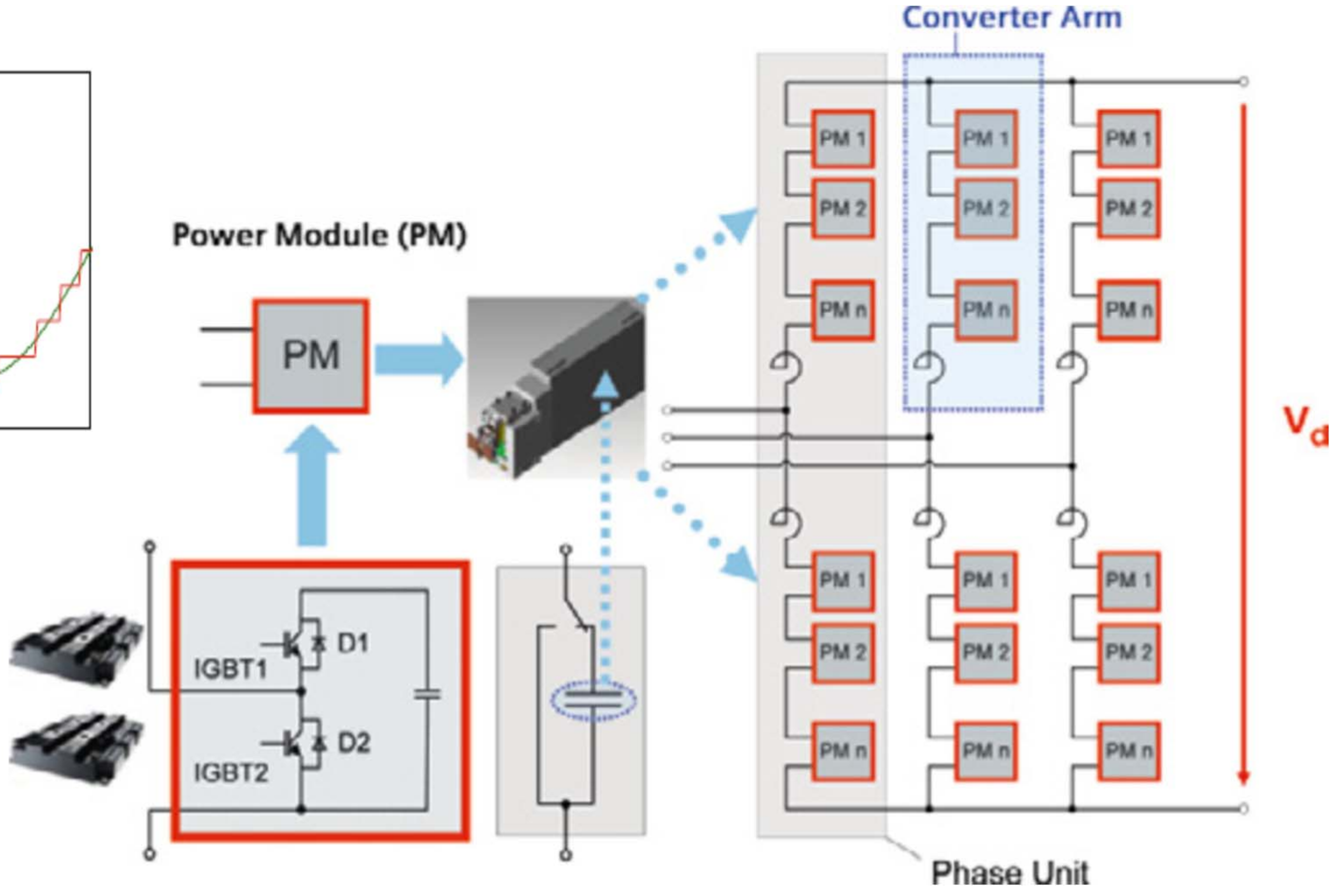


Types of MMC

Half-Bridge MMC 2009

Siemens diagram





Note: Filters not required

VSC Valves: MMC

Half-Bridge – Cascaded 2-level converter

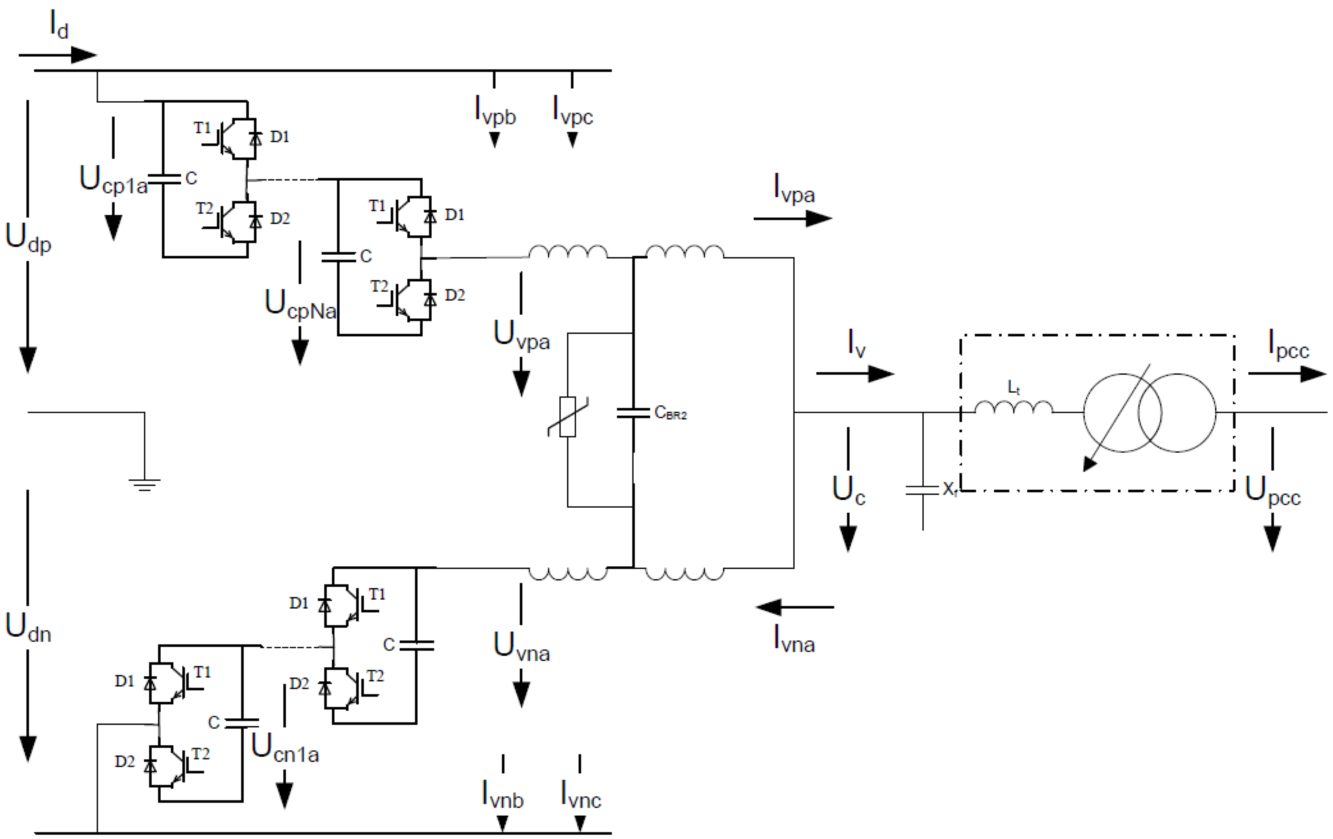
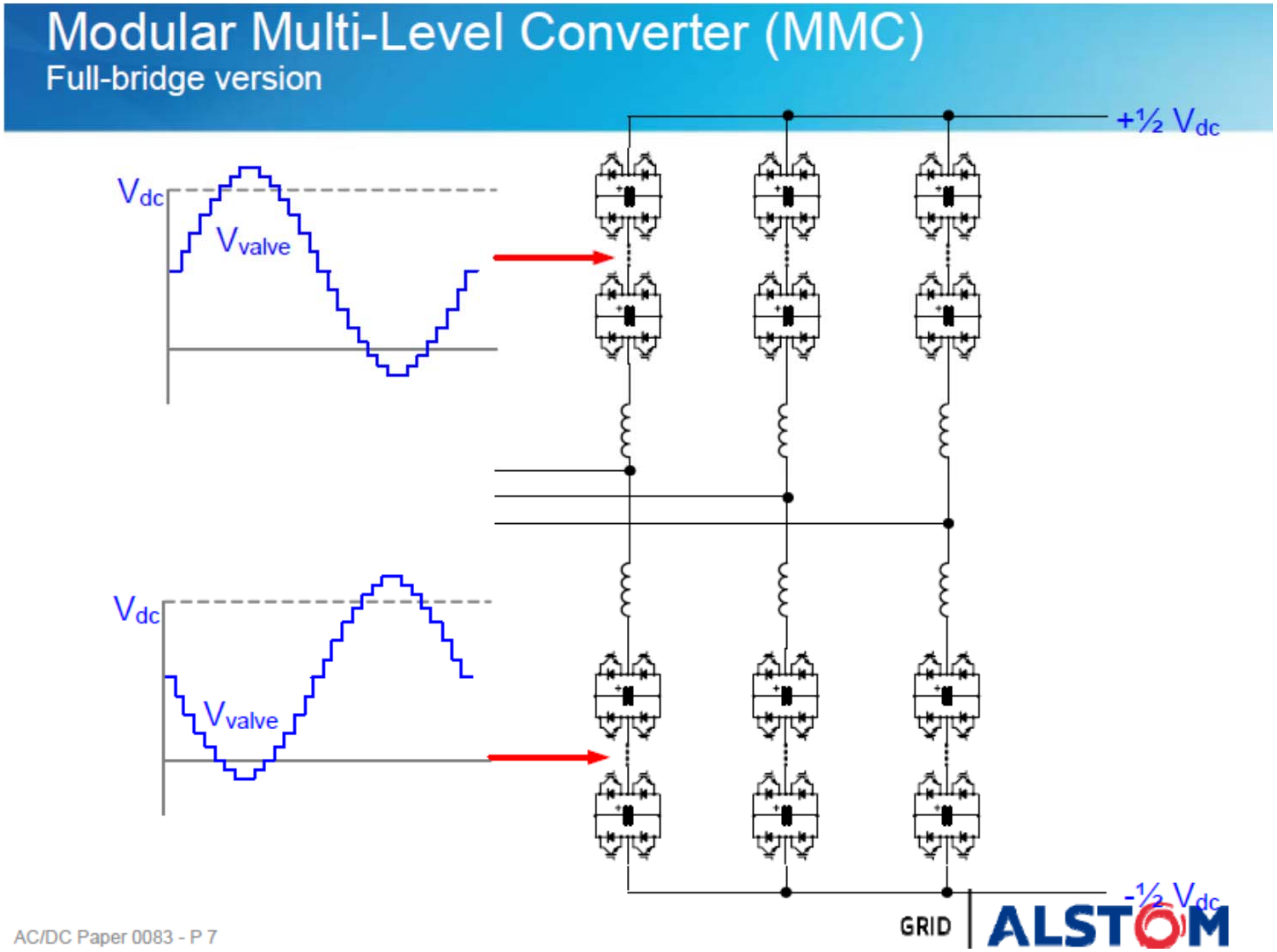


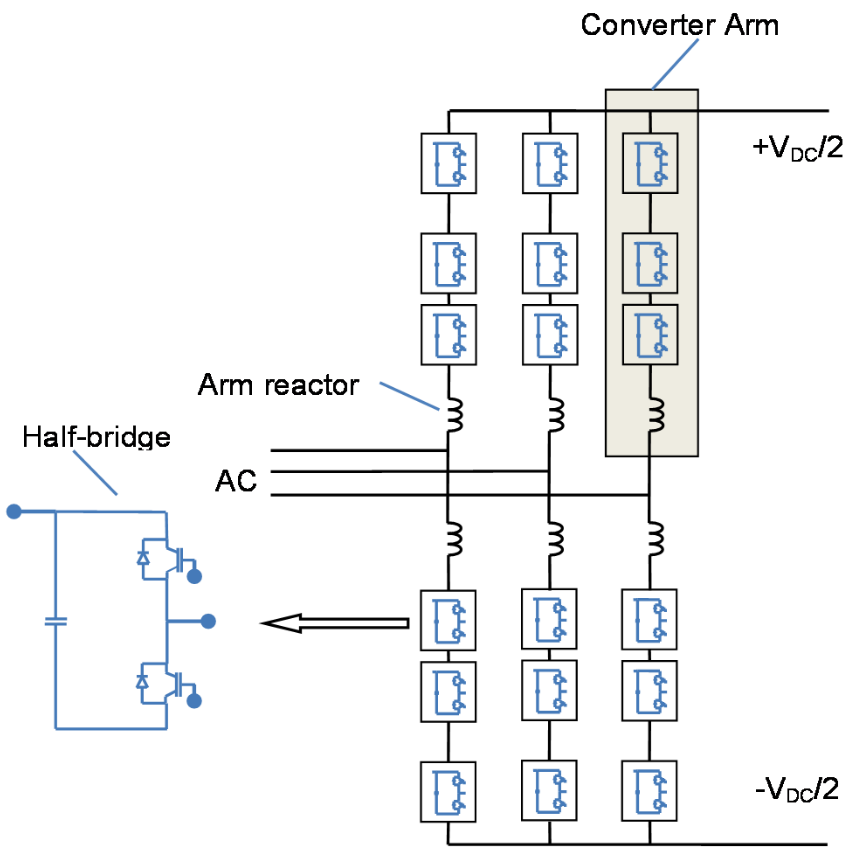
ABB diagram

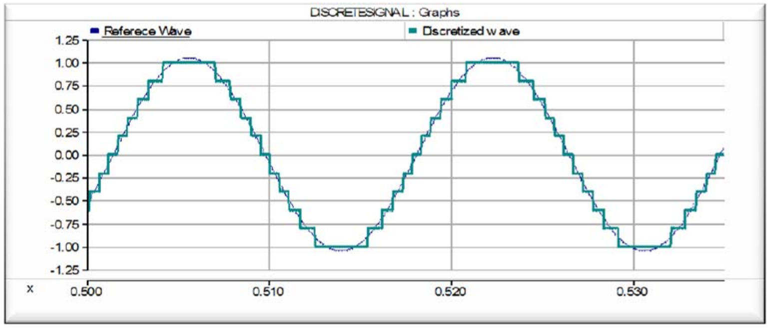
VSC Valves: MMC

Full- or H-bridge cells



Half-bridge MMC





Half-bridge MMC

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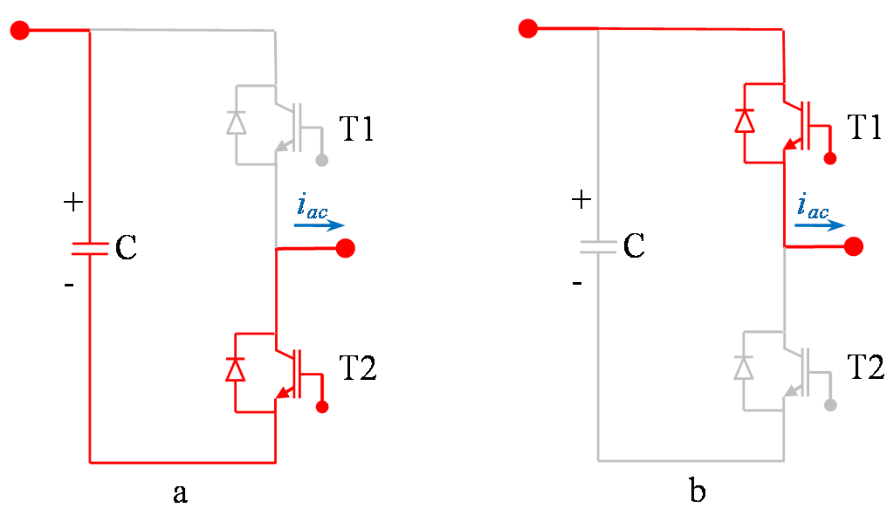
Three operating states in the half-bridge cell

State description	Gates
Insert +Vc	(T2)
Bypass capacitor	(T1)
Blocked	None
Forbidden	(T1,T2)



Half-bridge MMC

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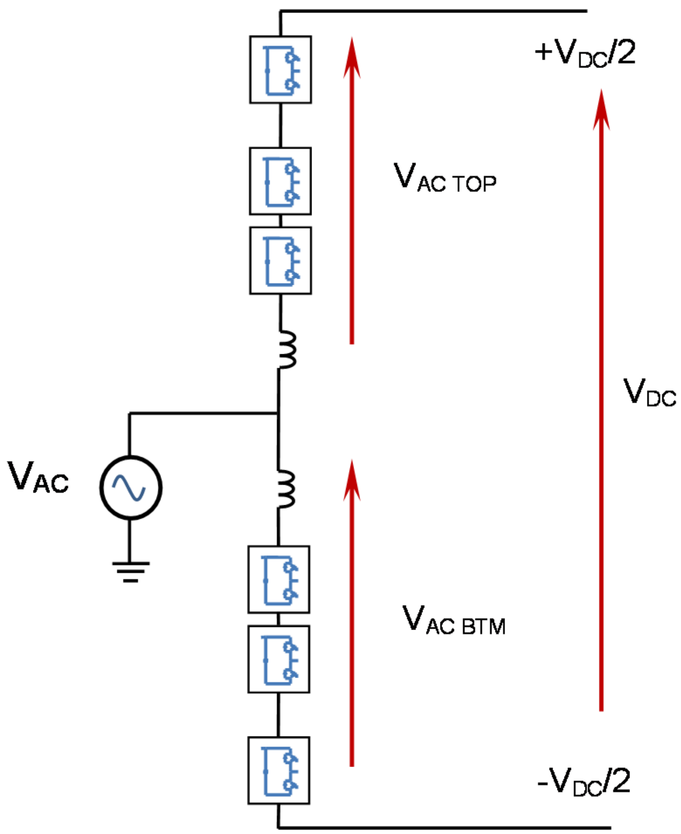
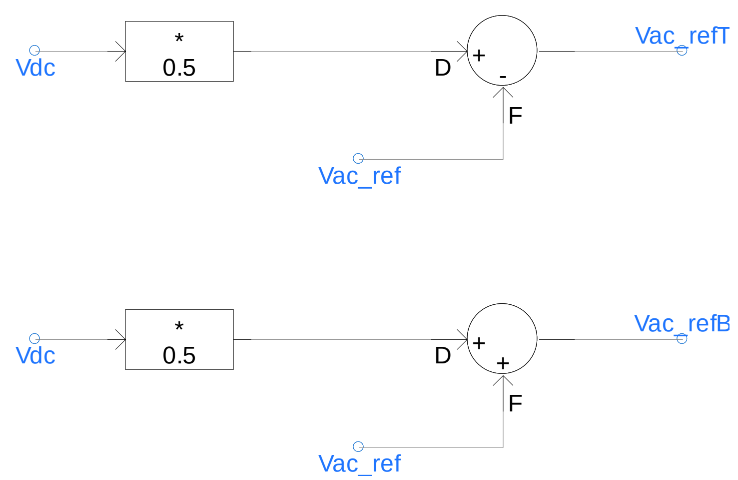


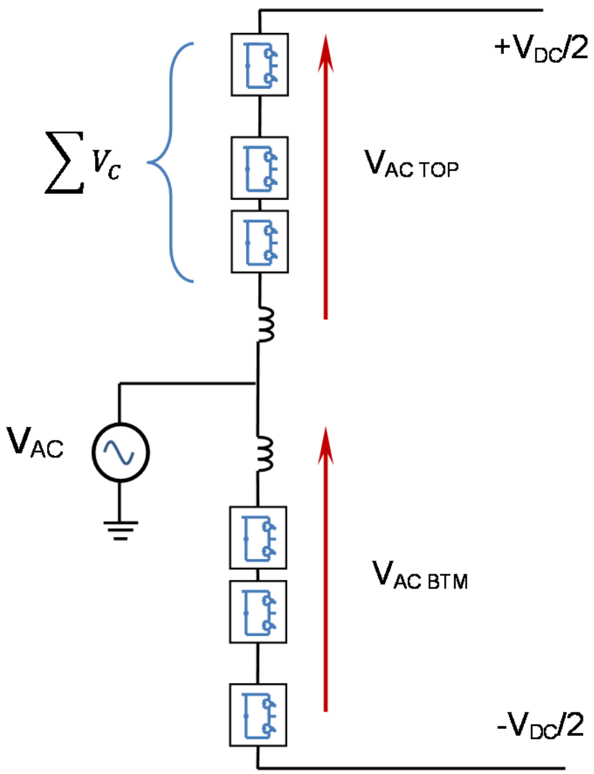
$$V_{AC\ TOP} = \frac{V_{DC}}{2} - V_{AC}$$

$$V_{AC\ BTM} = \frac{V_{DC}}{2} + V_{AC}$$



Note: Half-bridge CAN NOT generate $V_{DC} = 0$

Half-bridge MMC



Assuming modulating index = 1

$$V_{AC\ PEAK} = \frac{V_{DC}}{2}$$

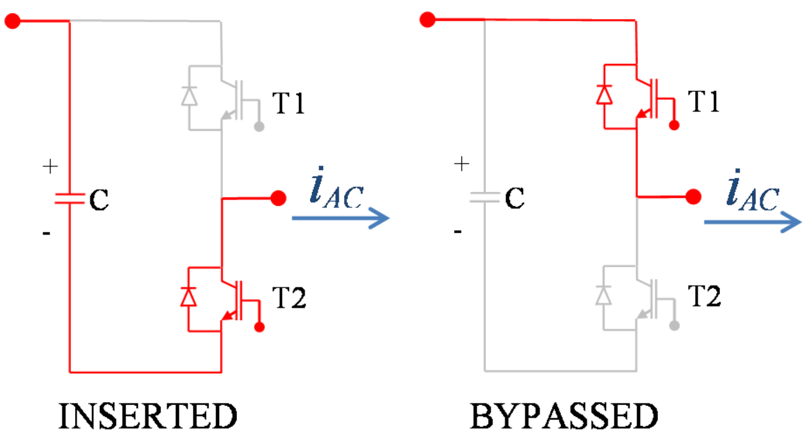
$$V_{AC\ TOP} = \frac{V_{DC}}{2} - V_{AC}$$

$$V_{AC\ BTM} = \frac{V_{DC}}{2} + V_{AC}$$

V_{AC}	$V_{AC\ TOP}$	$V_{AC\ BTM}$
$+V_{DC}/2$	0	V_{DC}
0	$V_{DC}/2$	$V_{DC}/2$
$-V_{DC}/2$	V_{DC}	0

$$\sum V_C = V_{DC}$$

Capacitor balancing: sorting method – Half-bridge cell



	$i_{ac} < 0$	$i_{ac} > 0$
Inserted cell	Discharges capacitor	Charges capacitor
Bypassed cell	Prevents discharging of capacitor	Prevents charging of capacitor

Capacitor balancing: sorting method – Half-bridge cell

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Measurements

Vcapacitors, Iac

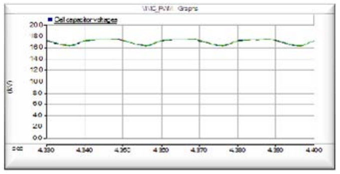
Ordering of capacitors by voltage

IGBT firing strategy PWM, Level switching

Request for insertion or bypass of a cell capacitor

Firing order according to table below

Balanced capacitor voltages



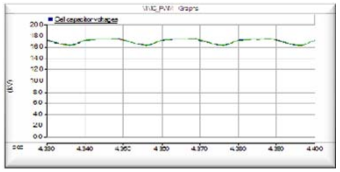
IGBT Firing orders

Action requested	$i_{ac} < 0$	$i_{ac} > 0$
Insert cell	Insert cell with highest voltage	Insert cell with lowest voltage
Bypass cell	Bypass cell with lowest voltage	Bypass cell with highest voltage

Low Level Controls

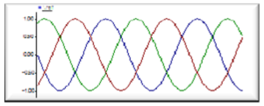
Stages

Half-bridge cell Capacitor balancing algorithm

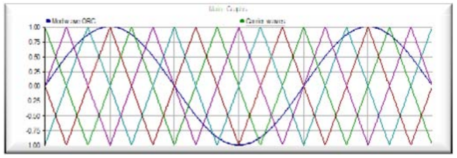


Balanced capacitor voltages

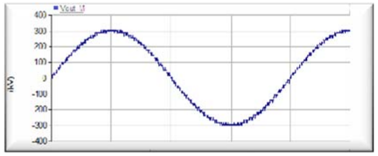
Reference voltage waves



IGBT firing strategy PWM, NLC, etc.



Sinusoidal(*) AC voltages



(*) or with harmonic content as required

H-bridge MMC (full-bridge)

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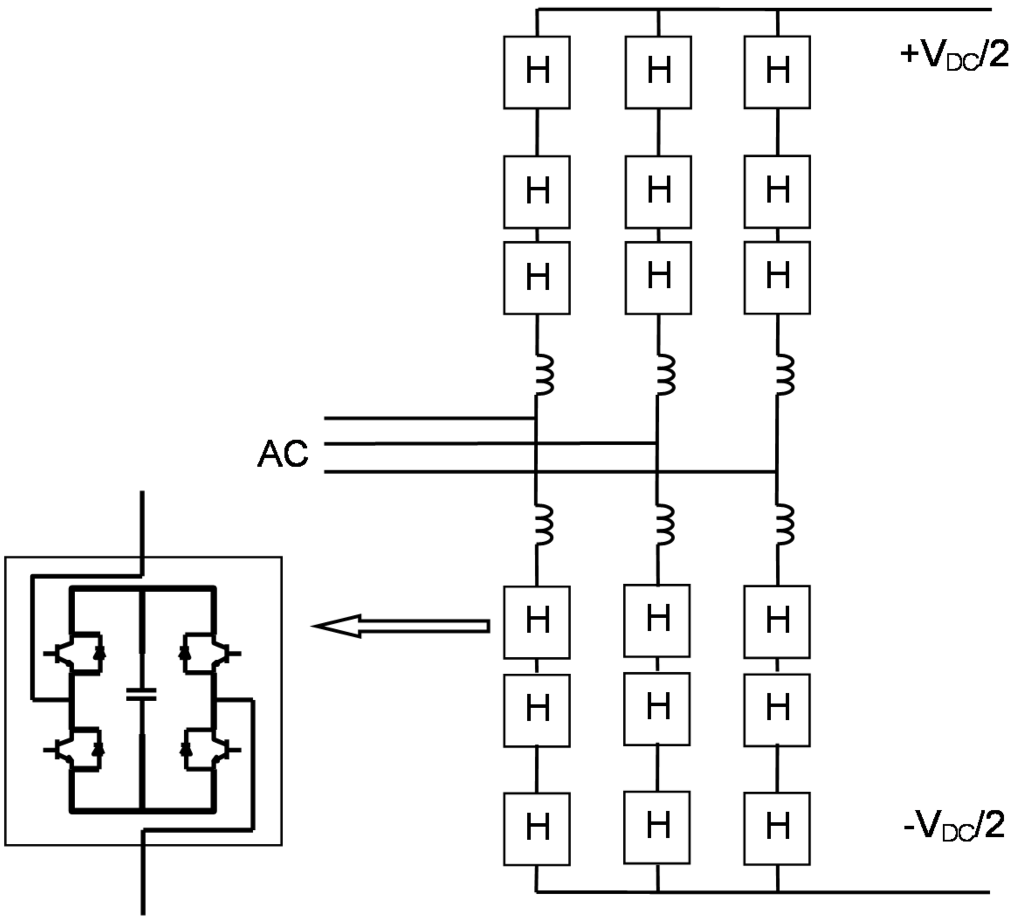
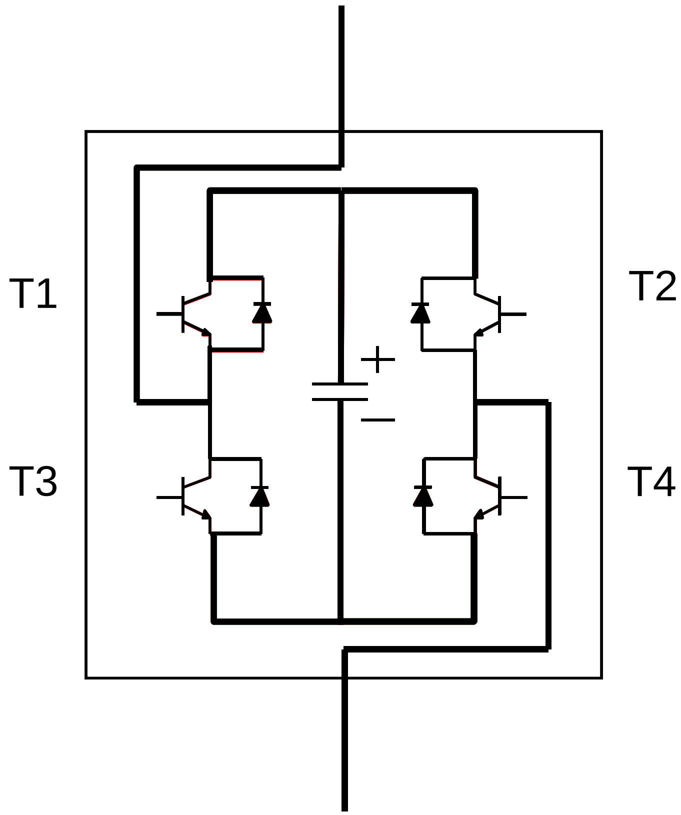


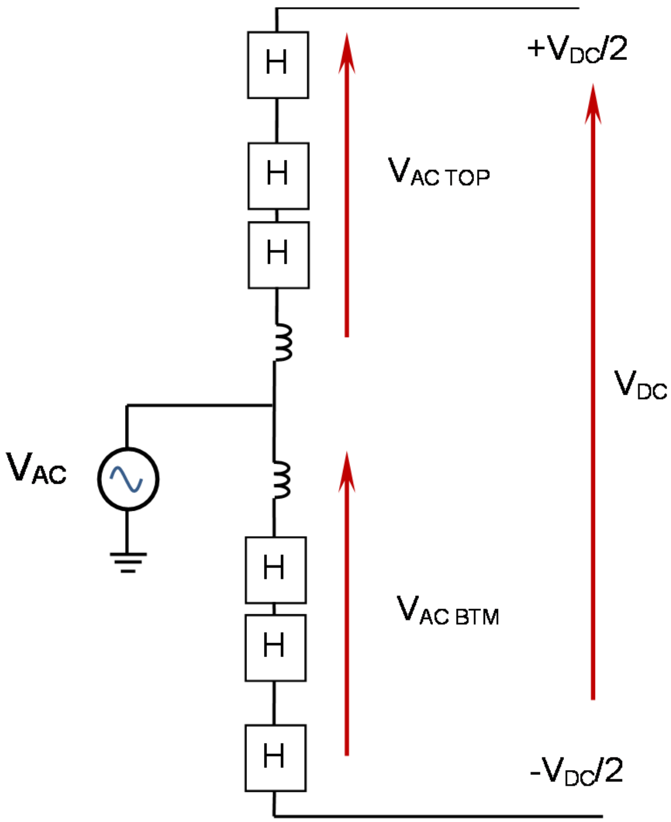
H-bridge

Four operating states

State description	Gates
Insert +Vc	(T1,T4)
Insert -Vc	(T3,T2)
Bypass capacitor	(T1,T2) or (T3,T4)
Blocked	None
Forbidden	(T1,T3) & (T2,T4)

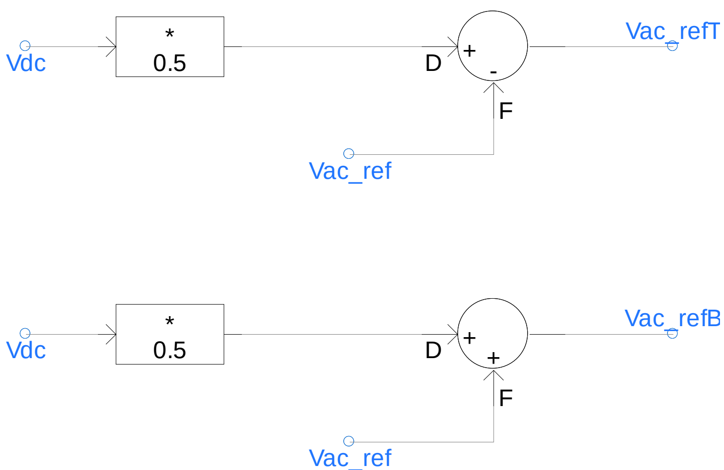


H-bridge



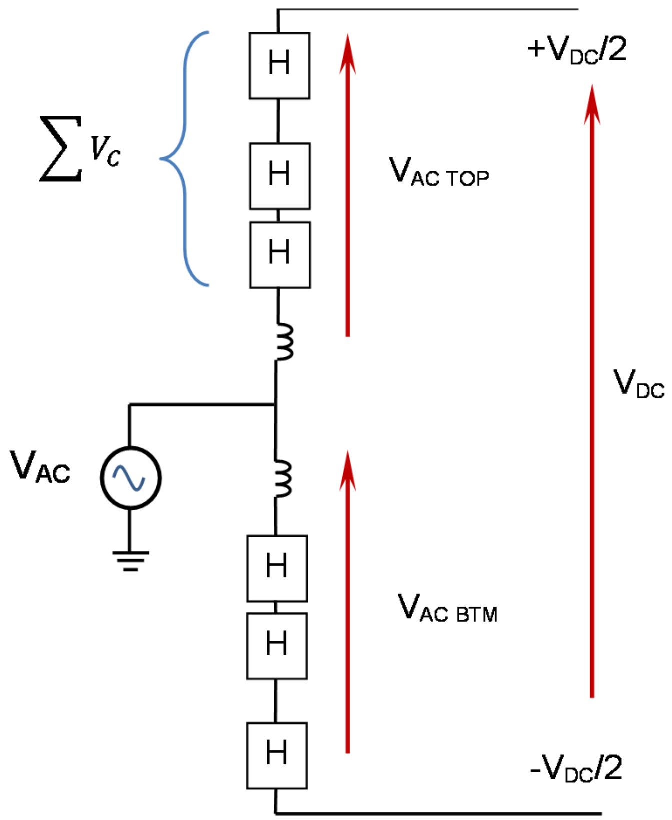
$$V_{AC\ TOP} = \frac{V_{DC}}{2} - V_{AC}$$

$$V_{AC\ BTM} = \frac{V_{DC}}{2} + V_{AC}$$



Note: H-bridge CAN generate $V_{DC} = 0$

Half-bridge MMC



Assuming modulating index = 1.25

$$V_{AC\ PEAK} = 1.25\frac{V_{DC}}{2}$$

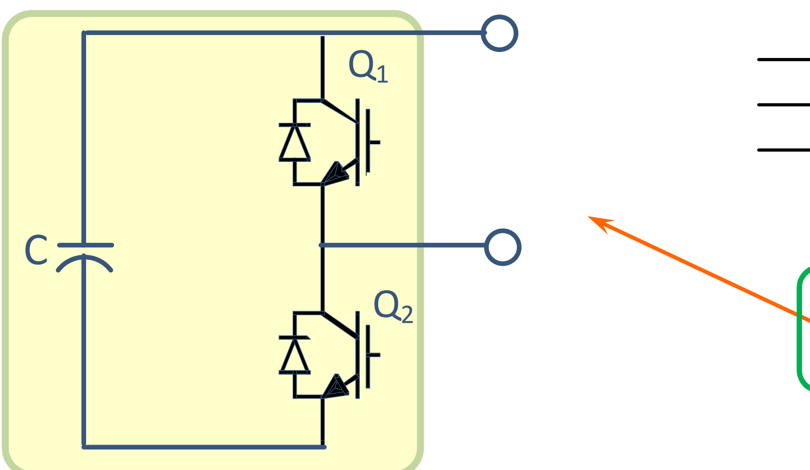
$$V_{AC\ TOP} = \frac{V_{DC}}{2} - V_{AC} \qquad V_{AC\ BTM} = \frac{V_{DC}}{2} + V_{AC}$$

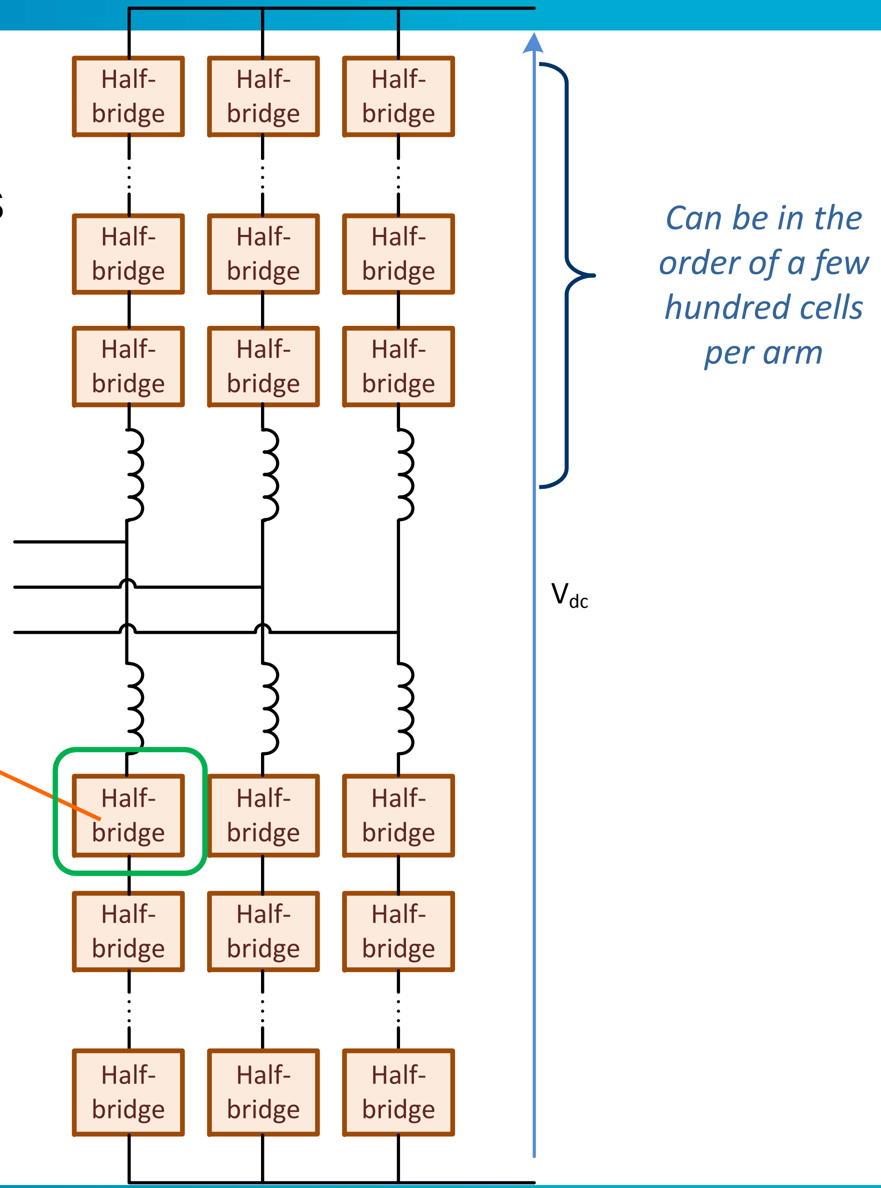
V_{AC}	$V_{AC\ TOP}$	$V_{AC\ BTM}$
$+1.25V_{DC}/2$	$-0.125V_{DC}$	$1.125V_{DC}$
$+V_{DC}/2$	0	V_{DC}
0	$V_{DC}/2$	$V_{DC}/2$
$-V_{DC}/2$	V_{DC}	0
$-1.25V_{DC}/2$	$1.125V_{DC}$	$-0.125V_{DC}$

$$\sum V_C = 1.125 \times V_{DC}$$

Modelling techniques: MMC valves

- Simulation of MMC VSCs can involve hundreds of nodes. This significantly reduces simulation speed.





Modelling techniques: MMC valves

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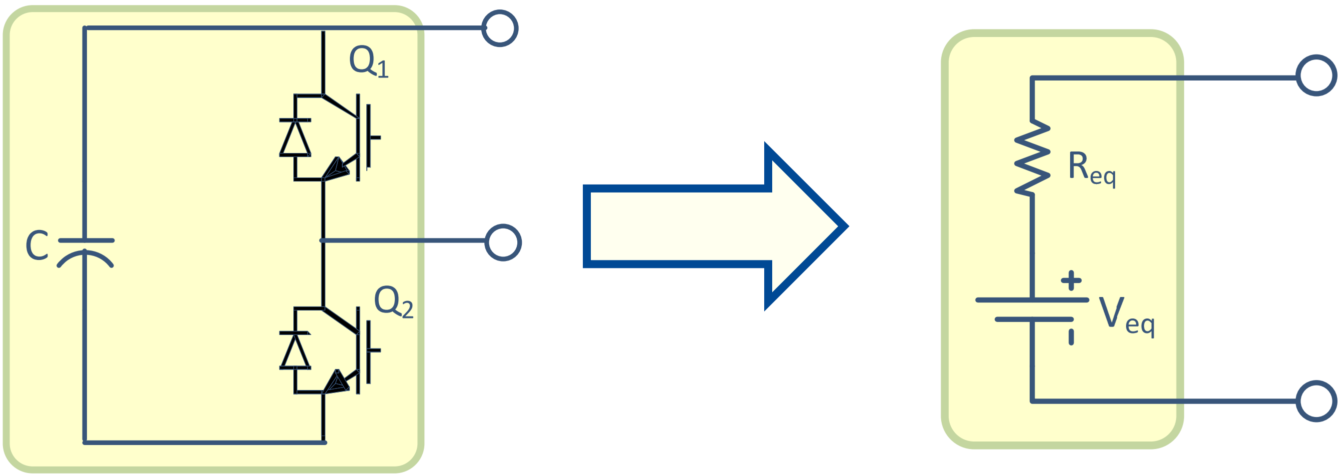
- Using Thevenin equivalent:
  (detailed equivalent model)

$$R_{eq} = R_1 \left[1 - \frac{R_1}{R_1 + R_2 + R_C} \right]$$

$$V_{eq} = \frac{R_1}{R_1 + R_2 + R_C} V_C$$



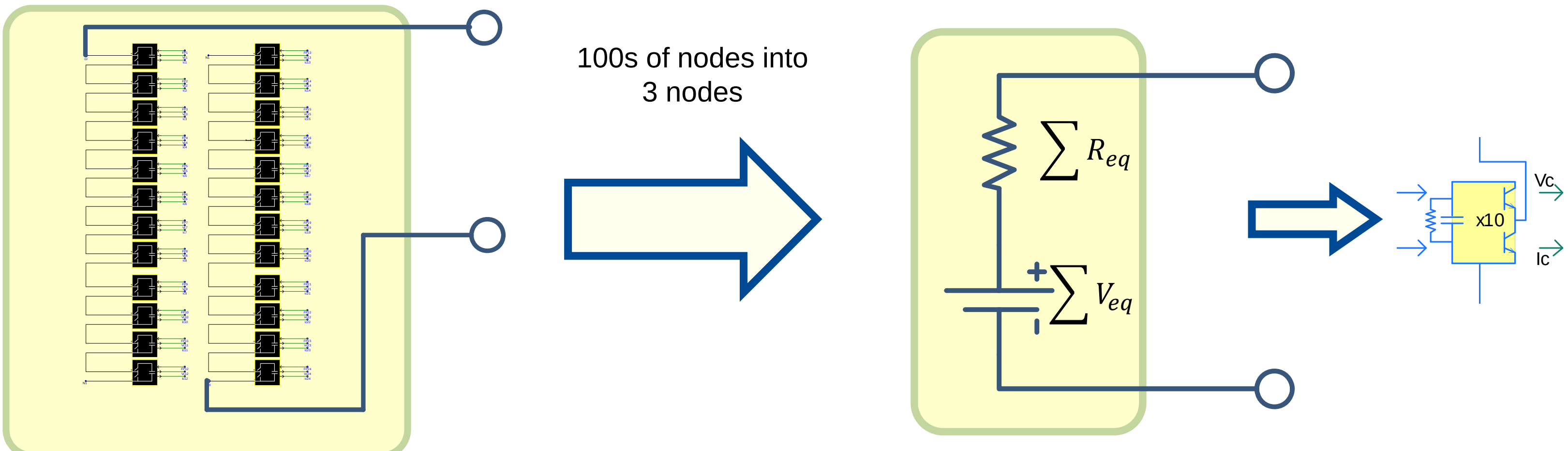
U. N. Gnanarathna, A. M. Gole, and R. P.Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," IEEE Transactions on Power Delivery, vol.26, no.1, pp.316-324, Jan. 2011

Modelling techniques: MMC valves

- Using Thevenin equivalent:
  (detailed equivalent model)

$$R_{eq} = R_1 \left[1 - \frac{R_1}{R_1 + R_2 + R_C} \right]$$

$$V_{eq} = \frac{R_1}{R_1 + R_2 + R_C} V_C$$



- This type of model is identified in CIGRE WB B4-57 as model Type-4
- This model is good for system wide studies and for most DC fault simulations

Start-up sequence

Converter 1: Grid-connected mode ⟶ Controls V_{dc} and Q (or V_{ac})

Converter 2: Grid-connected mode ⟶ Controls P and Q (or V_{ac}) – in black start mode

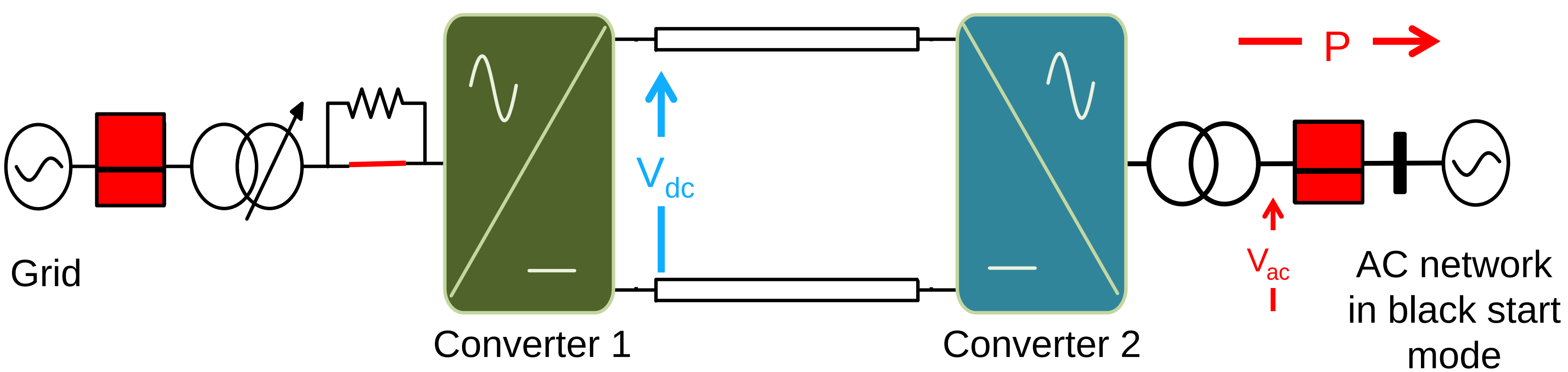
Converter 1

- Energize transformer & Pre-charge
- Bypass pre-insertion resistor
- Deblock converter 1
- Regulate V_{dc}

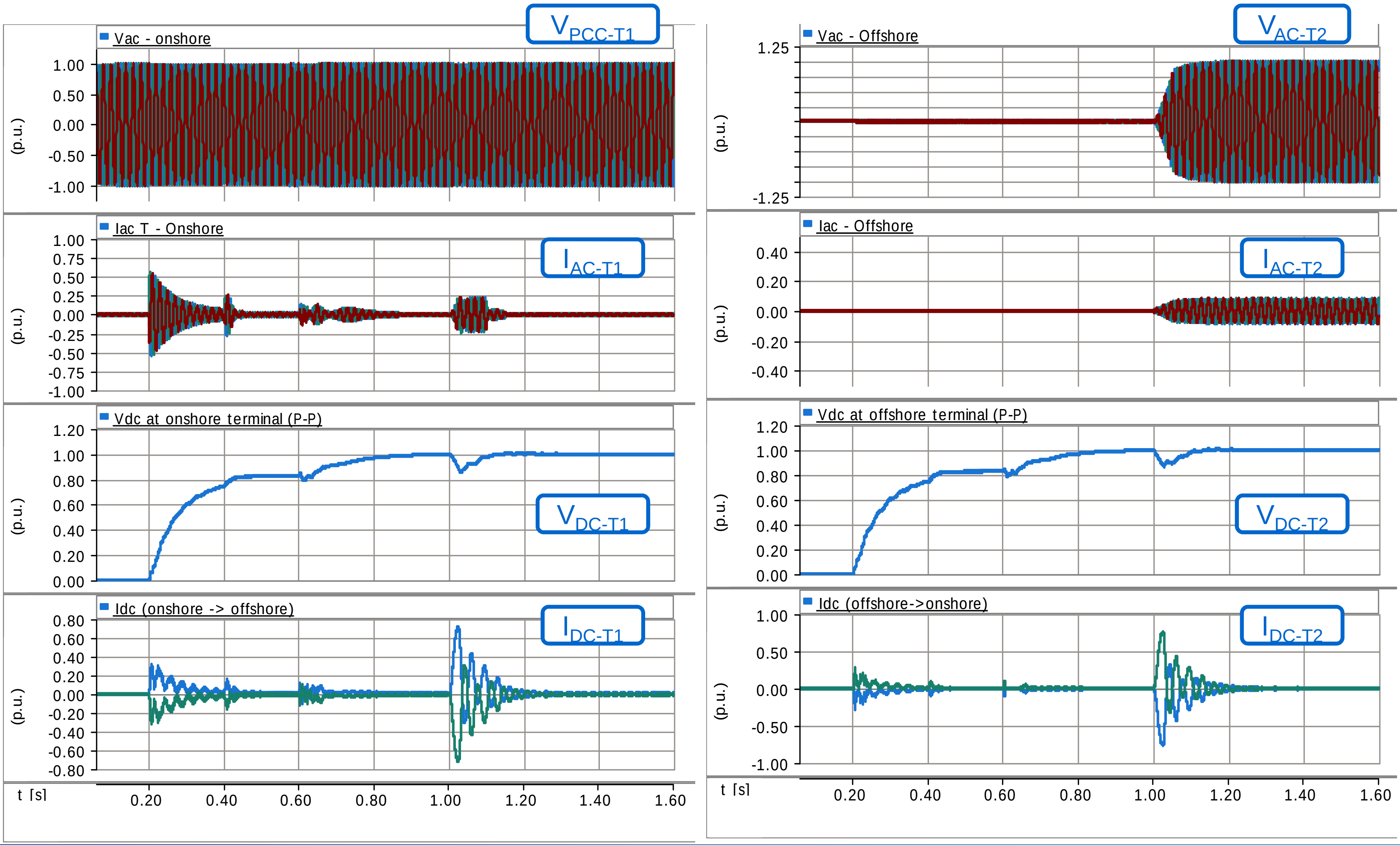
Converter 2

After V_{dc} is regulated:

- Deblock converter 2
- Regulate V_{ac}
- Ramp-up power transfer

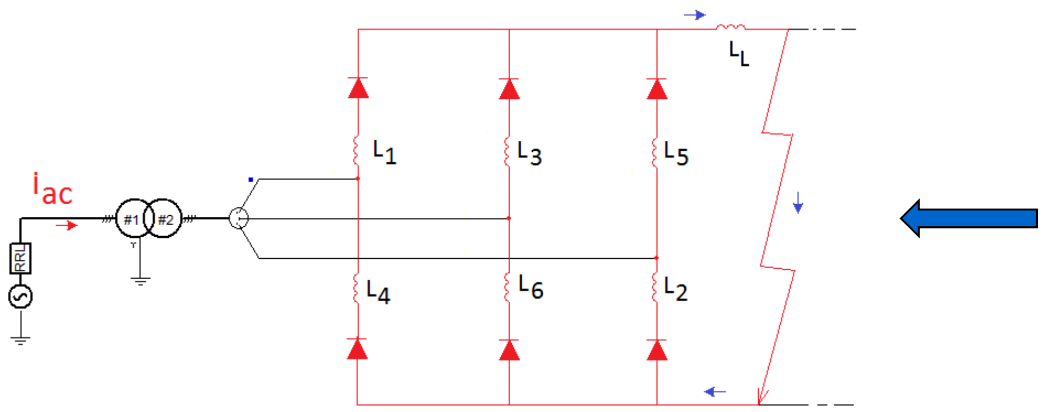


Start-up sequence



Half-bridge DC faults performance

- Sustained DC faults (unlike LCC)

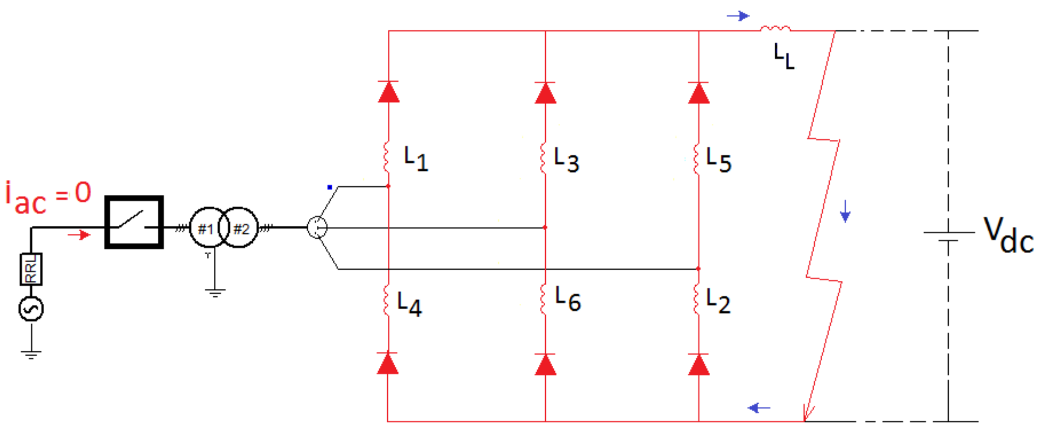


Applies to conventional 2-Level VSC and Half-bridge MMC

- Most systems (except one) use cables:
  - No need for fast re-energization
  - Cables experience low occurrence of faults
  - Fault clearing by opening AC breaker

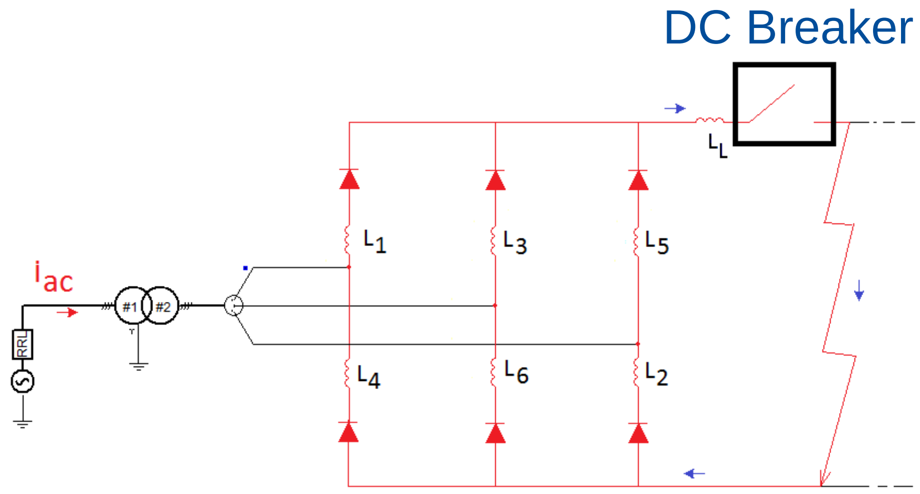
Half-bridge DC faults performance

- Most systems use cables:
  - No need for fast re-energization
  - Cables experience low occurrence of faults
  - Fault clearing by opening AC breaker



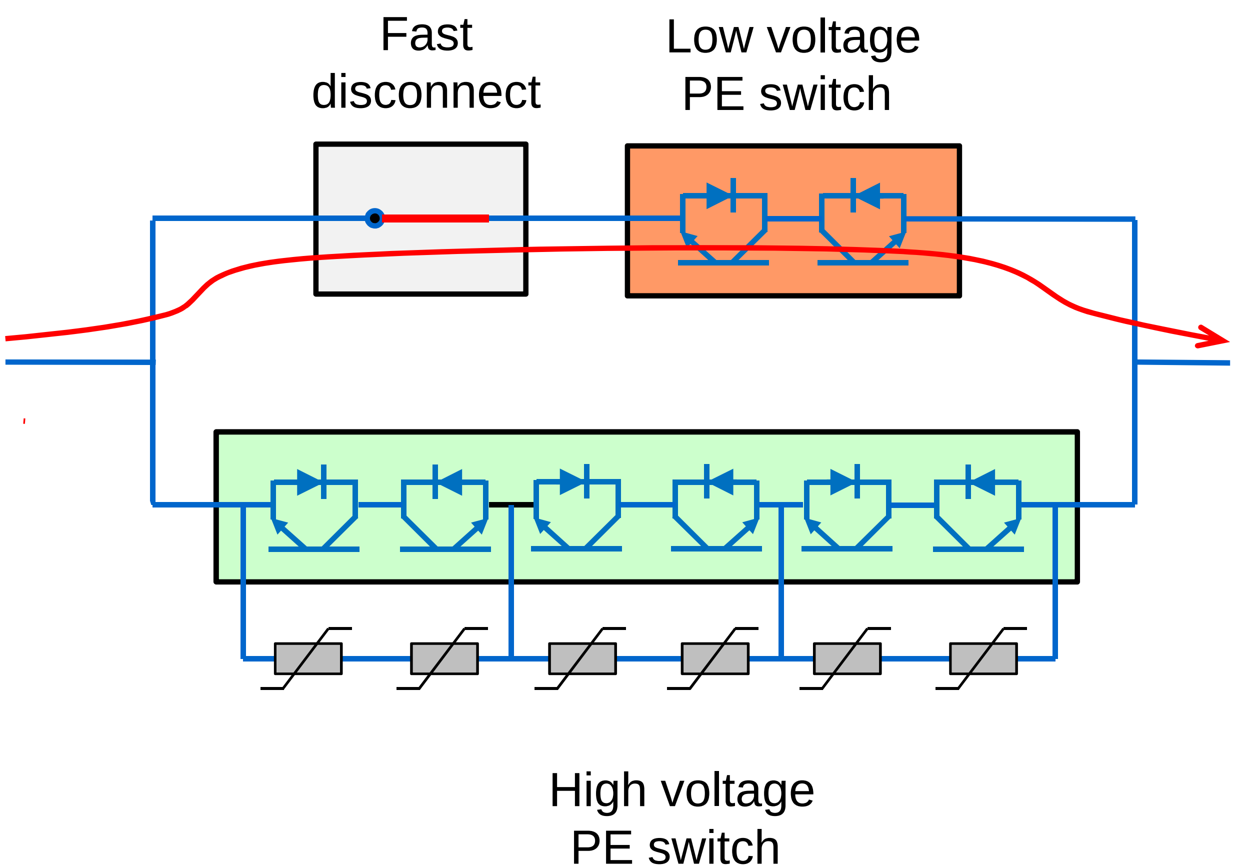
DC faults in VSC systems with Overhead Lines (OHL)

- High fault event frequency with OHL
- Need fast re-energization (re-closing) (400-500 ms) to prevent AC system movement
- DC breakers are required in order to achieve fast re-energization of DC system



Half-bridge DC faults performance

DC-Breakers

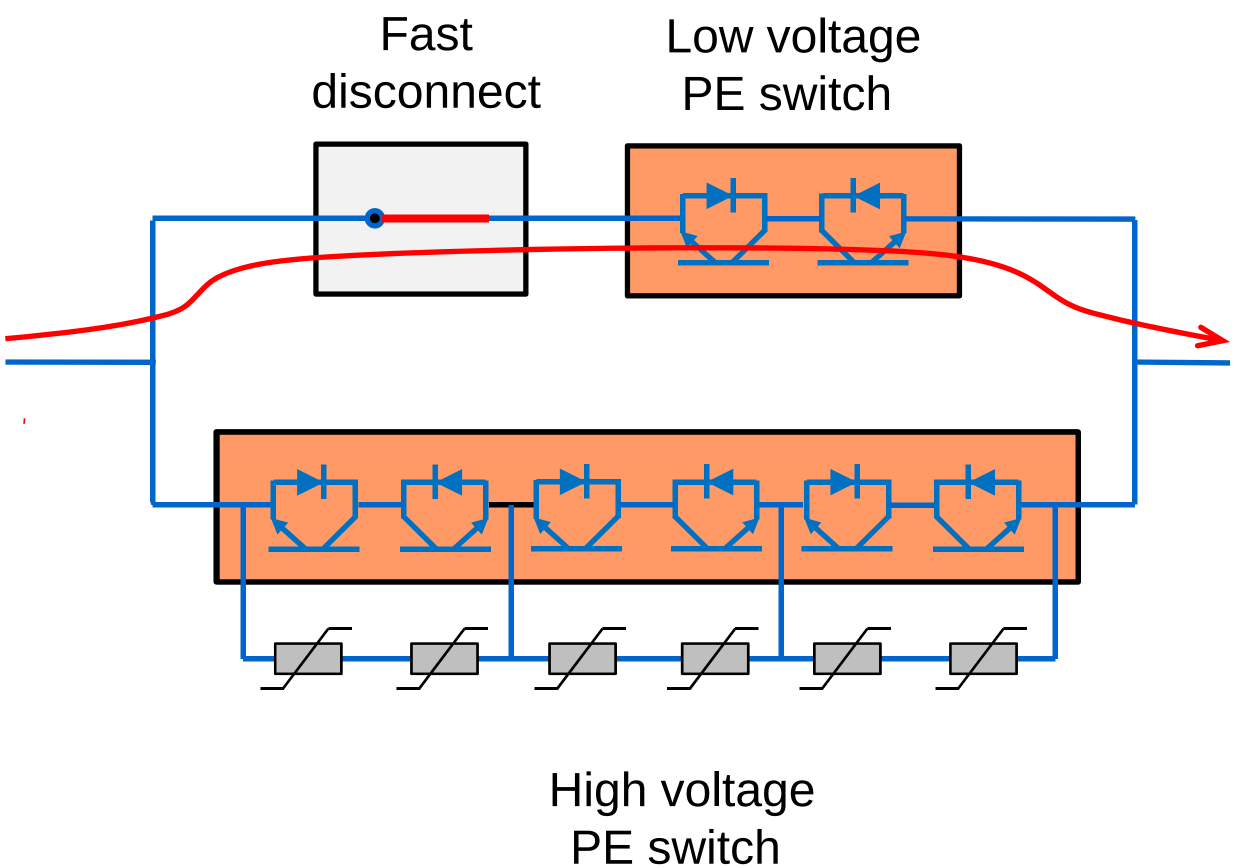


1. Overcurrent or DC fault under voltage front detected

Half-bridge DC faults performance

MANITOBA·HVDC RESEARCH CENTRE

DC-Breakers

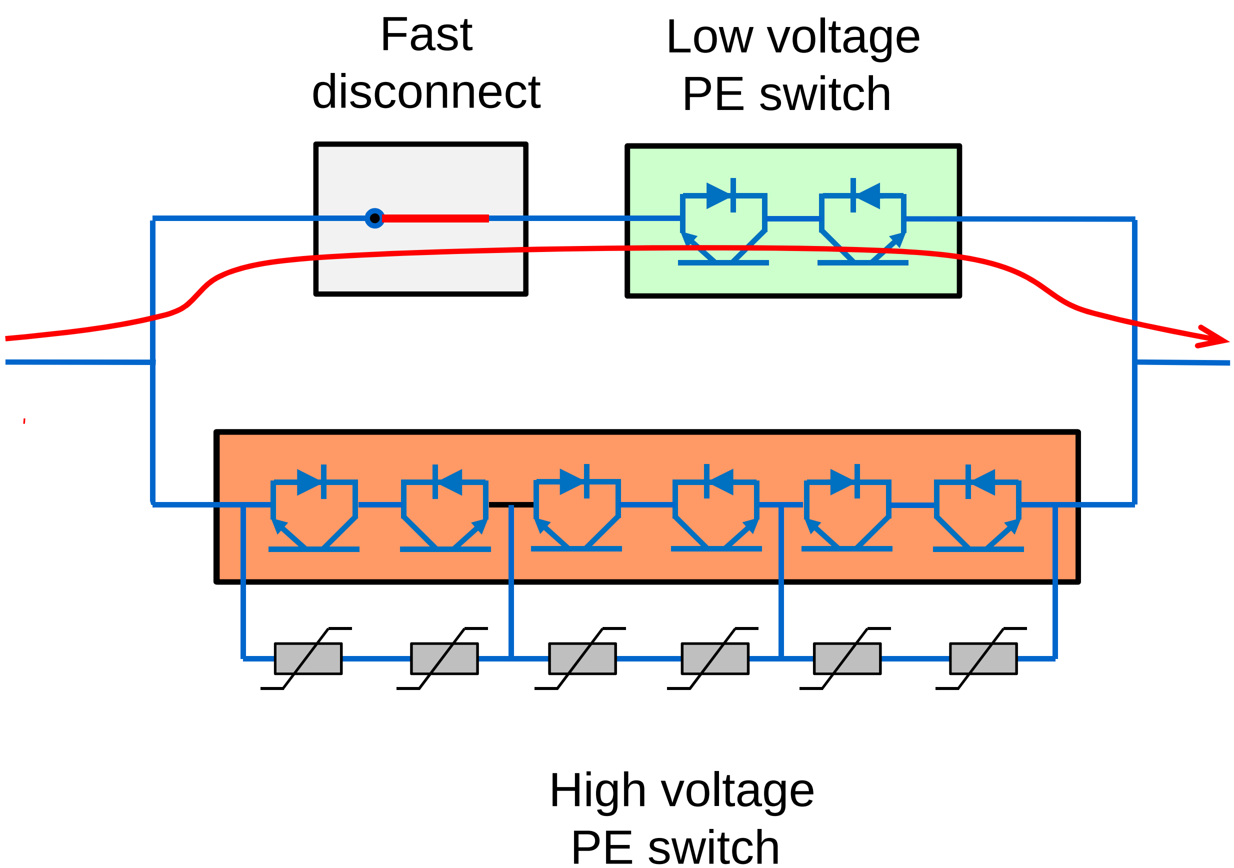


1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch

Half-bridge DC faults performance

MANITOBA-HVDC RESEARCH CENTRE

DC-Breakers

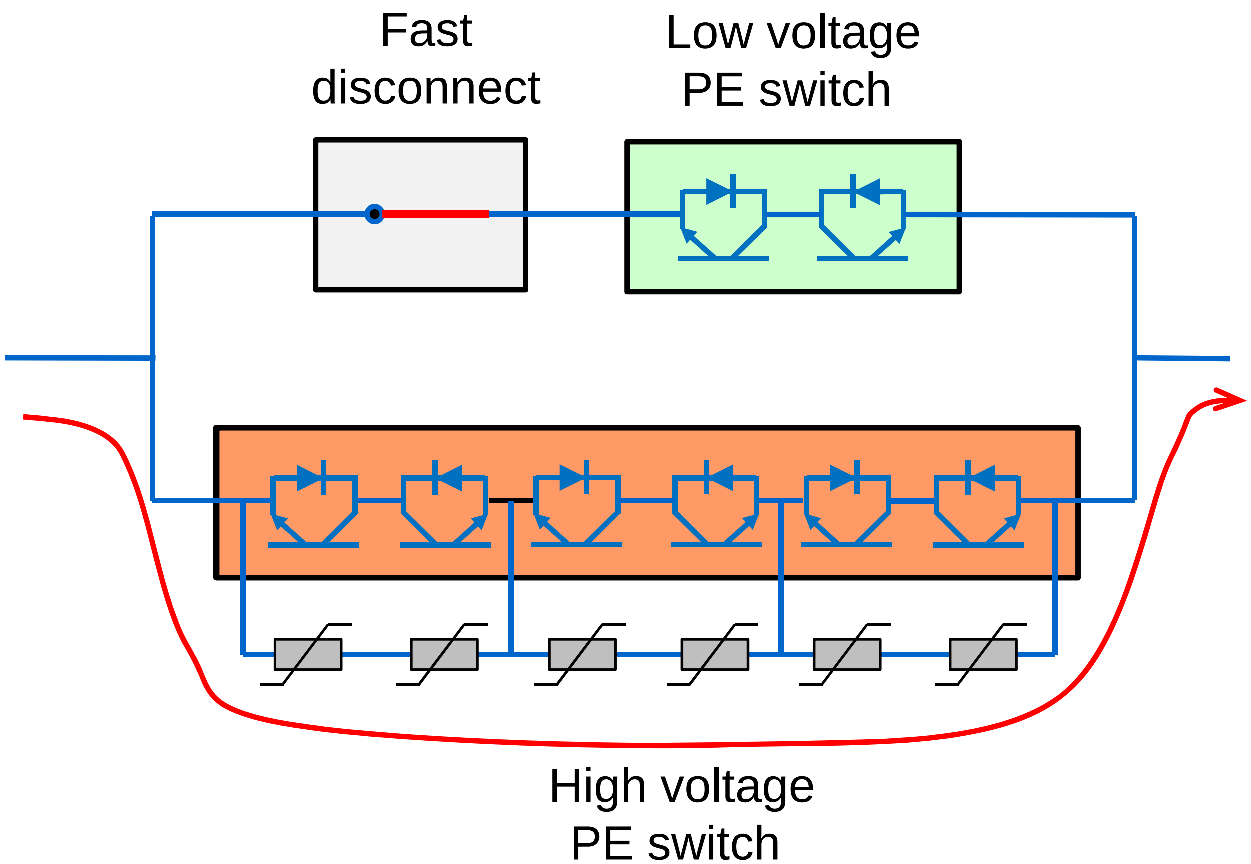


1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch
3. Open LV PE switch

Half-bridge DC faults performance

MANITOBA-HVDC RESEARCH CENTRE

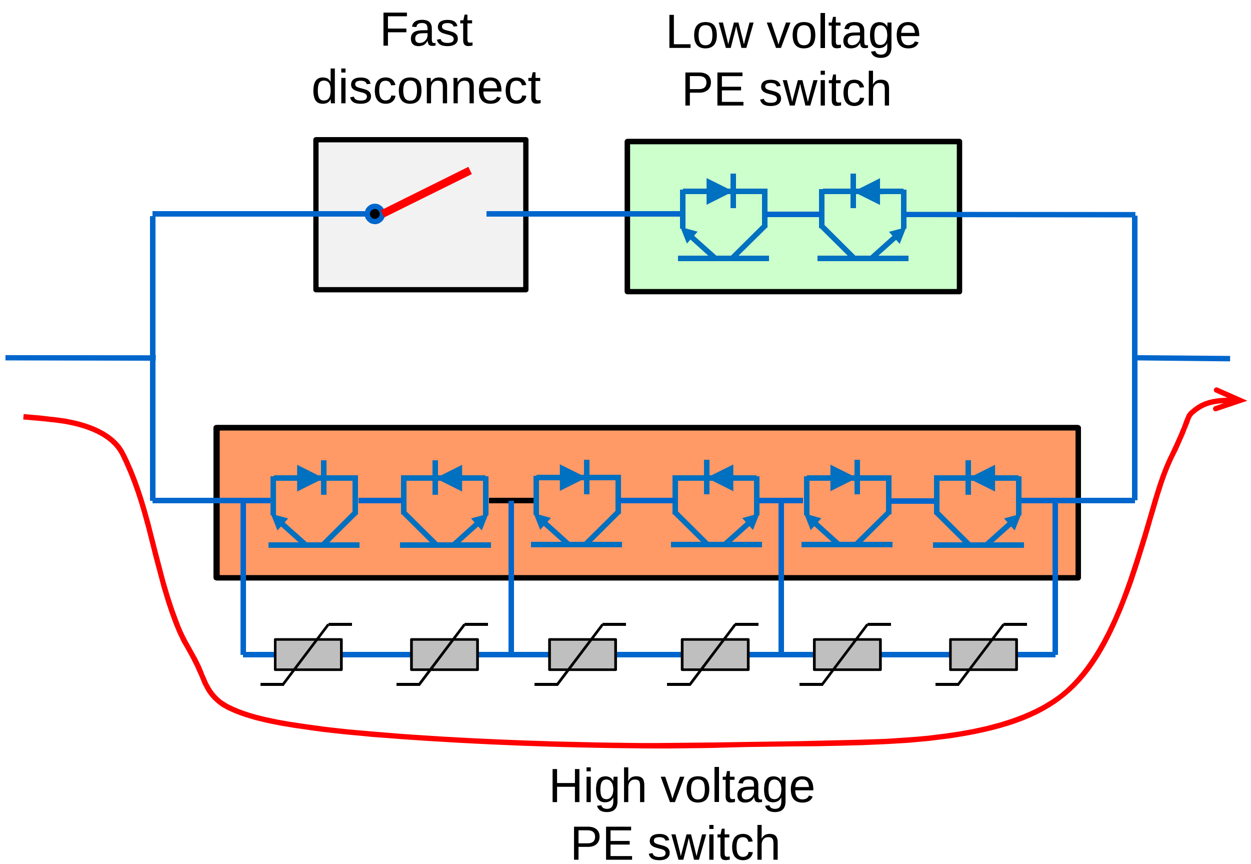
DC-Breakers



1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch
3. Open LV PE switch
4. Current transferred to HV PE switch

Half-bridge DC faults performance

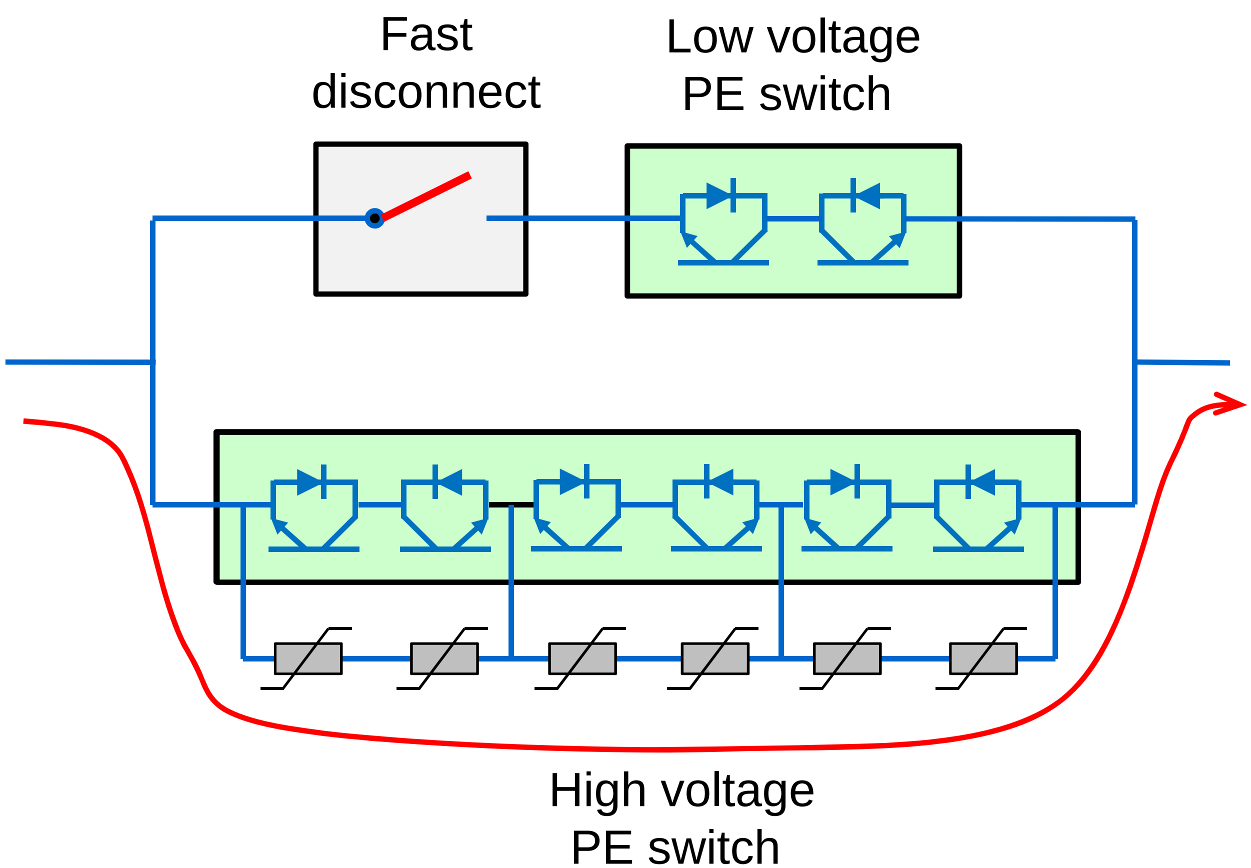
DC-Breakers



1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch
3. Open LV PE switch
4. Current transferred to HV PE switch
5. Open fast disconnect

Half-bridge DC faults performance

DC-Breakers

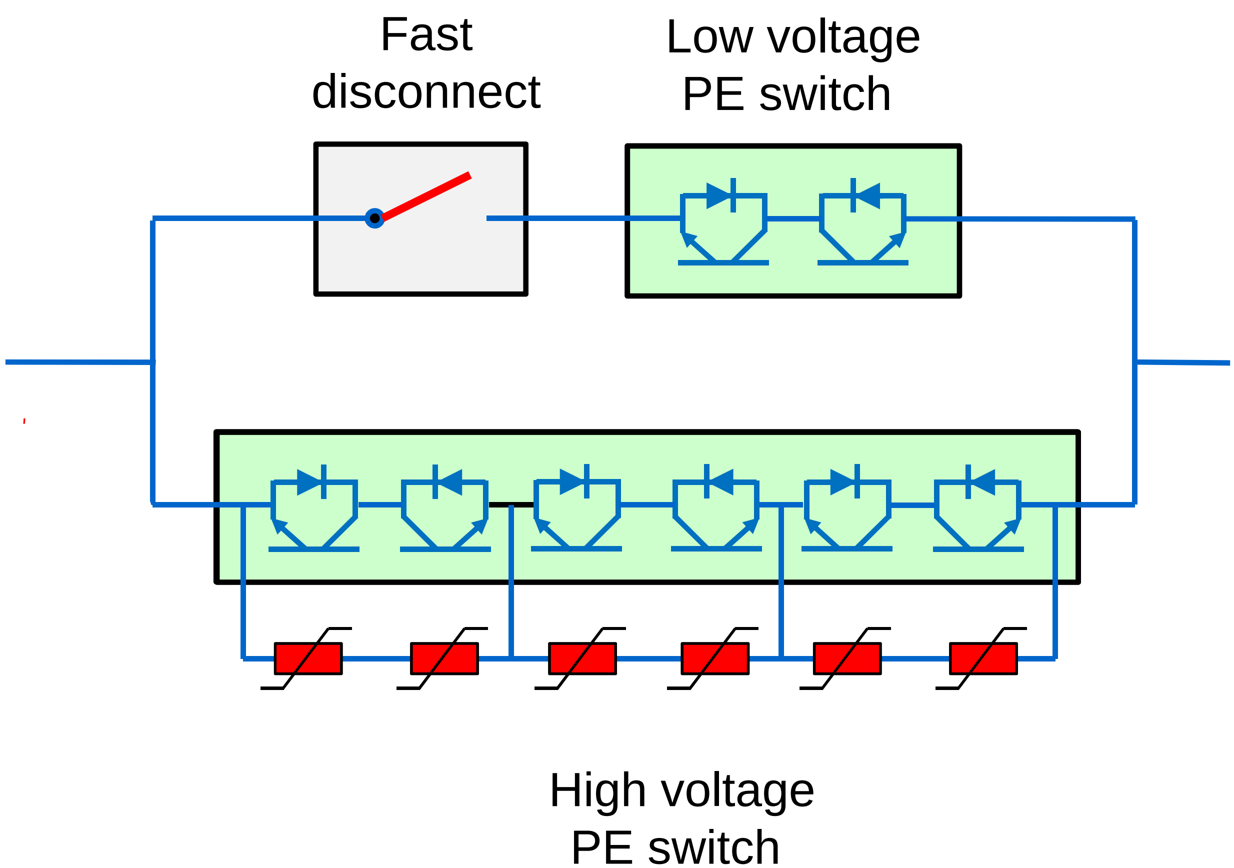


1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch
3. Open LV PE switch
4. Current transferred to HV PE switch
5. Open fast disconnect
6. Open HV PE switch

Half-bridge DC faults performance

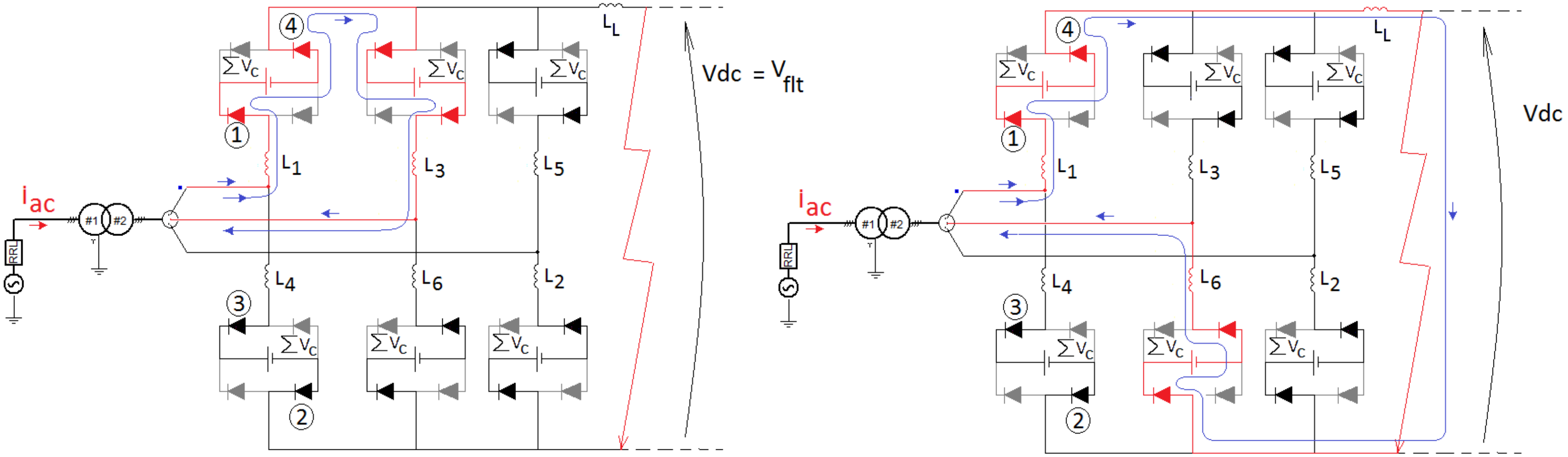
MANITOBA-HVDC RESEARCH CENTRE

DC-Breakers



1. Overcurrent or DC fault under voltage front detected
2. De-block HV PE switch
3. Open LV PE switch
4. Current transferred to HV PE switch
5. Open fast disconnect
6. Open HV PE switch
7. DC current extinguished & energy dissipated in arresters

Fault clearance in H-bridge VSC systems (by blocking)



$$|i_{AC}| \begin{cases} > 0 & if \;\; v_{AC\;l-l} \geq 2\sum_i k_i v_C \\ = 0 & otherwise \end{cases}$$

- Therefore Iac=0 after blocking since

$$V_{AC_{L-L\;pk}} = m\sqrt{3}V_{dc}$$

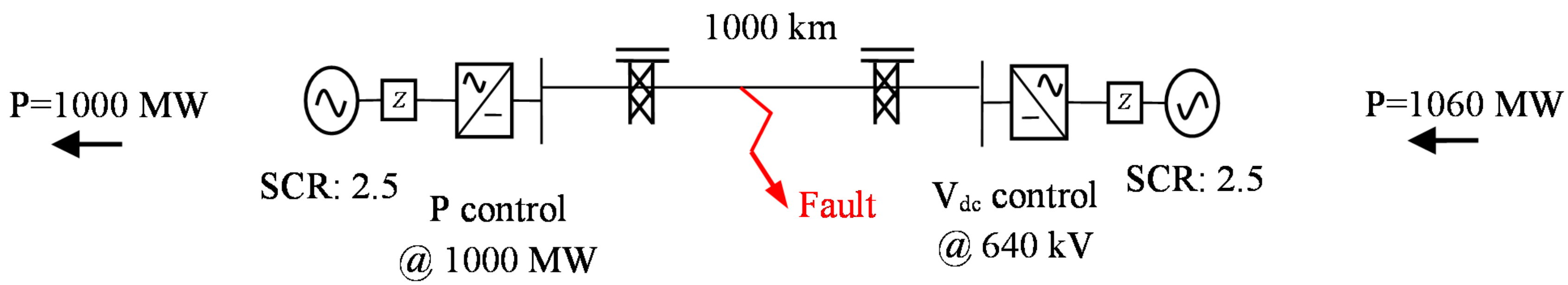
$$\sum v_c = V_{dc}$$

$$\Rightarrow$$

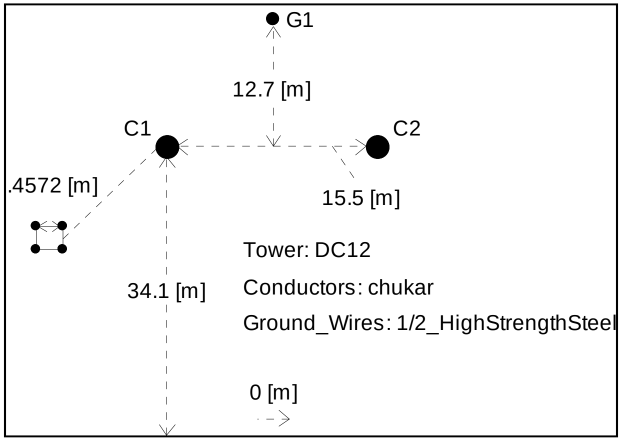
$$m\sqrt{3}V_{dc} \not\geq 2V_{dc}$$

Simulation of DC faults in a two-terminal system

System description



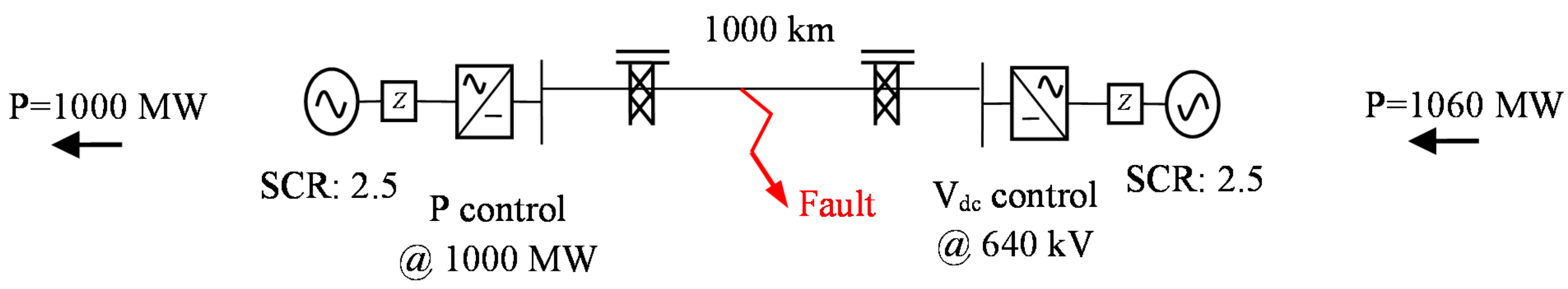
- T1: P control
- T2: Vdc control
- T1 & T2 in Vac control



TL Freq. dependent model

Simulation of DC faults in a two-terminal system

DC Faults applied

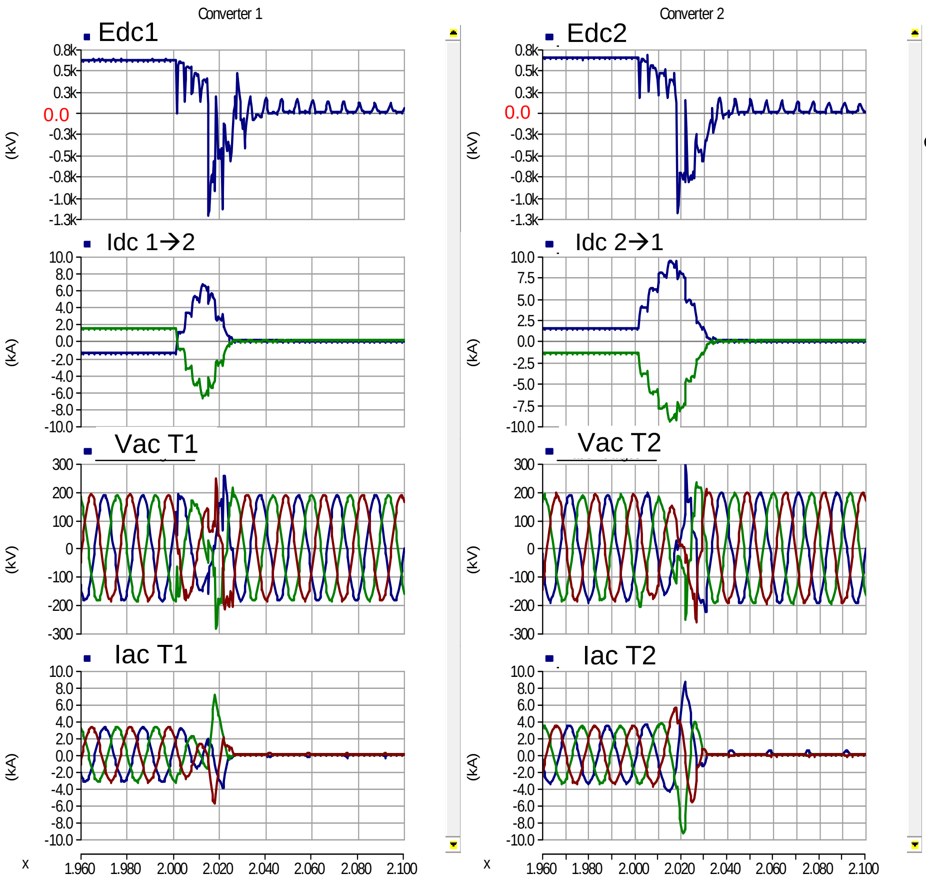


- At close and remote terminals
- Middle of the line
- Low impedance faults (0.1 ohm)

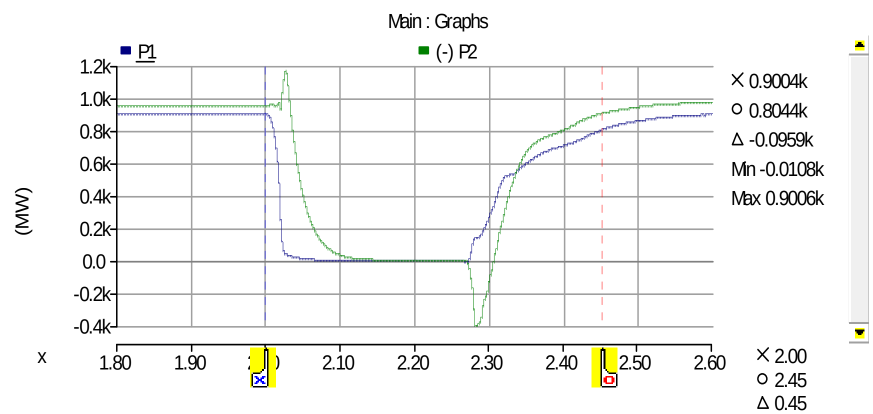
DC Faults detection

- Valve overcurrent (2.7 kA level)
- DC voltage drop (40% of diode rectifier voltage

Simulation of DC faults in a two-terminal system



- The total time to restore 90% power was 450ms
  - Including 200 ms de-ionization time



Three-terminal system: Demonstration setup

- Starting with the two-terminal system from CIGRE B4-57
- If time allows

Questions

- Please e-mail PSCAD Support at

  support@pscad.com